DIN EN 16602-70-12:2016-12 (E)

Space product assurance - Design rules for printed circuit boards; English version EN 16602-70-12:2016

Contents

Page

European foreword 12

Introduction 13

1 Scope 14

2 Normative references 15

3 Terms, definitions and abbreviated terms 16

3.1 Terms from other standards 16

3.2 Terms specific to the present standard 16

3.3 Abbreviated terms 24

4 Principles 26

4.1 Qualified PCBs 26

4.2 Manufacturing tolerances 26

4.3 Reliability of design 26

5 Design review and MRR 28

5.1 Overview 28

5.2 Documentation 28

6 General design and production requirements 30

6.1 Reliability of design 30

6.2 Choice of materials and build-up 30

6.2.1 Overview 30

6.2.2 Material selection 33

6.3 Selection of the PCB manufacturer 33

6.4 Traceability and marking 33

7 Rigid PCBs 34

7.1 PCB build-up 34

7.1.1 General 34

7.1.2 Copper styles 34

7.1.3 Dielectric thickness 36

7.2 PCB dimension 39

7.3 Thickness of PCB 39
7.3.1 General 39
7.3.2 Polyimide PCB 40
7.3.3 Epoxy PCB 40
7.3.4 Number of copper layers in PCB 40
7.3.5 Aspect ratio of vias 40
7.4 Track width and spacing 41
7.4.1 General 41
7.4.2 Manufacturing tolerances for width and spacing 41
7.4.3 External layers 42
7.4.4 Normal pitch tracks on internal layers 43
7.4.5 Fine pitch tracks on internal layers 44
7.4.6 Routing to AAD footprint on internal layers 45
7.5 Pad design 46
7.5.1 Non-functional pad removal 46
7.5.2 Pad dimensions 46
7.5.3 Non-circular external pads 48
7.6 Copper planes in rigid PCB 49
7.7 Design considerations for the prevention of sliver and peelable 50
7.8 PCB surface finish 50
7.8.1 Metallization 50
7.8.2 Solder mask 51

8 Flex PCBs 52

8.1 Overview 52
8.2 Dynamic applications 52
8.3 PCB build-up 52
8.3.1 General 52
8.3.2 Dielectric materials 52
8.3.3 Copper cladding 53
8.3.4 Copper planes in flex PCB 53
8.4 Track design 54
8.5 Through holes 55
8.5.1 Annular ring 55
8.5.2 Vias and pads 56
8.5.3 Tear drop pad for flex PCB 56
8.6 Bending radius 57
8.6.1 Overview 57
8.6.2 General 57

8.7 Sculptured flex PCB 58
8.7.1 Overview 58
8.7.2 General 58
8.7.3 Copper foil dimensions for build-up 58
8.7.4 Connection finger 59
8.7.5 Through-holes 60
8.7.6 Bending radius 61

9 Rigid-flex PCBs 62
9.1 Overview 62
9.2 General 62
9.3 Build-up 63
9.4 Cover layer 64
9.5 Interface of rigid part and flexible part 64
9.6 Pads 64

10 Thermal rules and heat sinks 65
10.1 Overview 65
10.2 General requirements 65
10.3 Specific requirements for external heat sink 65
10.3.1 Overview 65
10.3.2 Construction of the interface between PCB and heat sink 65
10.3.3 Dimensional requirements 66
10.4 Specific requirements for internal heat sink 68
10.4.1 General 68
10.4.2 Cu thickness and type 68
10.4.3 CIC and Molybdenum inserts 69
10.4.4 Dimensional requirements 69

11 HDI PCBs 71
11.1 Overview 71
11.2 Justification 71
11.3 Microvia technology 71
11.4 Microvias 72
11.4.1 Build-up of microvia layers 72
11.4.2 Design of microvias 74
11.4.3 Pad design for microvia 74
11.4.4 Annular ring for microvias 75
11.5 Core PCB for HDI 75
11.5.1 General build-up 75

11.5.2 Annular ring on vias for fine pitch footprint 76
11.5.3 Track width and spacing on external layers....77
11.5.4 Track width and spacing on internal layers for impedance control and routing to AAD 77
11.5.5 Track width and spacing on internal layers for differential pair routing within the footprint of 1,0 mm pitch AAD....78
11.5.6 Aspect ratio of vias for footprint of AAD with 1 mm pitch....79

12 PCBs for high frequency applications....81

12.1 Material selection....81
12.2 Build-up of RF PCB 81
12.3 Embedded film resistors 81
12.4 Thickness of RF PCB 83
12.5 Track width and spacing....83
12.5.1 External layers....83
12.5.2 Internal Layers....84
12.6 Pad design....84
12.6.1 Pad dimensions 84
12.6.2 Non-functional pads....84
12.7 Surface finish....84
12.8 Profiled layers and vias 84

13 Electrical requirements for PCB design 86

13.1 Overview....86
13.2 General....87
13.3 PCB drying 87
13.4 Electrical characteristics 87
13.5 Floating metal 88
13.6 Current rating....88
13.6.1 Overview....88
13.6.2 Requirements for temperature increment....89
13.6.3 Requirements for the model IPC-2152 for current rating....89
13.6.4 Amendments to the model from IPC-2152 90
13.7 Provisions to prevent open circuit failure on critical tracks 91
13.7.1 Overview....91
13.7.2 Routing 92
13.8 Voltage rating 92
13.8.1 Overview....92
13.8.2 General requirements....92
13.8.3 Spacing on flex and rigid-flex laminate....94

13.8.4 Conformal coating 95
13.9 Double insulation design rules for critical tracks 96
13.9.1 Overview 96
13.9.2 Critical nets 96
13.9.3 Prevention of short circuit 96
13.10 Insulation distance of combined requirements on rigid PCB 101
13.11 Controlled impedance tracks 106
13.11.1 Definitions specific to controlled impedance 106
13.11.2 General rules 106
13.11.3 Microstrip and stripline 106
13.11.4 Line impedance termination for end-to-end configuration 107
13.11.5 Line impedance termination for multidrop configuration 107
13.12 Digital PCB 108
13.12.1 Overview 108
13.12.2 Zone management and routing 108
13.12.3 Criticality of digital signals 109
13.13 Analog PCB 110
13.13.1 Overview 110
13.13.2 Criticality of analog signals 110
13.13.3 Routing and shielding 111
13.14 Mixed analog-digital PCB 112

14 Design for assembly 113

14.1 Overview 113
14.2 General 113
14.3 Placement requirements 114
14.3.1 Conductive patterns 114
14.3.2 Components 115
14.3.3 Component pads 117
14.3.4 Fan out of SMT pads 118
14.3.5 Fan out of PTH 120
14.4 Specific requirements for fused tin-lead finish 121
14.5 Dimensional requirements for SMT foot print 121
14.5.1 Overview 121
14.5.2 General 122
14.5.3 Bipolar components 123
14.5.4 SOIC components 124
14.5.5 J-leaded components 125
14.5.6 LCC components 126

14.5.7 Flat pack components....128
14.5.8 AAD components....129
15 Design of test coupon....130
15.1 Design rules for test coupon....130
15.2 Test coupon design....130
Annex A (normative) PCB definition dossier - DRD....133
A.1 DRD identification....133
A.1.1 Requirement identification and source document....133
A.1.2 Purpose and objective....133
A.2 Expected response....133
A.2.1 Scope and content....133
A.2.2 Special remarks....139
A.2.3 Example figures....139
Annex B (normative) PCB manufacturing dossier – DRD....144
B.1 DRD identification....144
B.1.1 Requirement identification and source document....144
B.1.2 Purpose and objective....144
B.2 Expected response....144
B.2.1 Scope and content....144
B.2.2 Special remarks....145
Annex C (informative) Example of capability list of PID....146
Annex D (informative) Track current rating computation methodology....148
D.1 Introduction of the three models....148
D.1.1 Overview....148
D.1.2 Formulae for the three models....149
D.1.3 Example of current rating....150
D.2 Track current rating computation based on IPC-2152....150
D.3 Track current rating computation based on CNES/QFT/IN.0113....154
D.4 Track current rating computation based on IPC-2221A....158
Annex E (informative) Example of calculation of PTH pad dimensions....162
Annex F (informative) Prevention of resin starvation and cracks....164
F.1 Prevention of resin cracks.....164
F.2 Prevention of resin starvation....164
Annex G (informative) Example of MRR checklist....166
Bibliography....170

Figures

Figure 3-1: Simplified build-up of HDI PCB 20
Figure 3-2: Projected peak-to-peak insulation distance 23
Figure 7-1: Example of automated fine pitch routing and possible improvements 45
Figure 7-2: Comparison between circular and oblong pads showing annular ring and the centre of the hole misregistered with the centre of the pad 48
Figure 7-3: Grid copper plane with openings 49
Figure 7-4: Example of peelable (left) and sliver (right) 50
Figure 8-1: Clearance of tracks on flex PCBs. 54
Figure 8-2: Tracks on flex, defining termination and bending zones. 55
Figure 8-3: Teardrop reinforcement of terminal pads in flex PCB. 56
Figure 8-4: Bending radius of assembled flex 57
Figure 8-5: Sculptured flex circuit 58
Figure 8-6: Build-up of sculptured flex circuit 59
Figure 8-7: Connection finger of sculptured flex circuit 60
Figure 8-8 Side view of a component hole for sculptured flex 61
Figure 9-1 Example of a build-up of a 6 layer symmetric rigid-flex 62
Figure 10-1: Lay out of heat sink and PCB 67
Figure 10-2: drilling holes and slots in internal heat sink 70
Figure 10-3: Angle of intersection of overlapping holes 70
Figure 11-1: Build-up of HDI PCBs with staggered (left) and stacked (right) microvia. 72
Figure 11-2: Dimple on a microvia 74
Figure 11-3: Tear drop pad design 76
Figure 11-4: Example of routing two differential pair tracks between vias in a footprint of an AAD with 1,27 mm pitch. 78
Figure 11-5: Example of routing two differential pair tracks between vias in a footprint of an AAD with 1 mm pitch. 80
Figure 13-1: Cross section of PCB with insulation distances. 87
Figure 13-2: Example of double insulation by increasing distance in X,Y and by not superimposing copper on adjacent layers 100
Figure 13-3: Example of double insulation by increasing distances in X,Y and by using two insulators in Z direction. 100
Figure 13-4: Edge coupled differential striplines 107
Figure 14-1: Illustration of surface pattern to adjacent surroundings 115
Figure 14-2: Illustration of component placing on PCB w.r.t. adjacent surrounding 116
Figure 14-3: Illustration of pad placing on PCB with respect to adjacent surroundings 118
Figure 14-4: Fan out from SMT pad to via 119

Figure 14-5: Example of point symmetric AAD footprint....120
Figure 14-6: Track width (I_c) ratio to PTH pad (D) diameter. 120
Figure 14-7: Track length (Lc) between soldering pad of PTH (D_1) and via pad (D_3)....121
Figure 14-8:Illustration of bipolar component pads 123
Figure 14-9: Illustration of SOIC component pads 124
Figure 14-10: Illustration of J-leaded component pads 125
Figure 14-11: Illustration of LCC component pads....126
Figure 14-12: Illustration of FP and QFP component pads 128
Figure 14-13: Illustration of AAD component pads....129

Figure A-1 : Example of PCB mechanical layout....139
Figure A-2 : Example of a drilling drawing....140
Figure A-3 : Example of a table indicating as-designed plated hole diameters....141
Figure A-4 : Example of build-up data....142
Figure A-5 : Example of the archive file with CRC 143
Figure D-1 : Comparison between CNES and IPC-2152 current rating at 5°C increase....149
Figure D-2 : IPC-2152: Current rating [A] vs cross sectional area [mm^2] in double log scale151
Figure D-3 : IPC-2152: Track width [mm] vs cross sectional area [mm^2]....151
Figure D-4 : IPC-2152: Current rating based on Figure D-2, range 0-25 A....152
Figure D-5 : IPC-2152: Current rating based on Figure D-2, range 0-10 A....152
Figure D-6 : IPC-2152: Current rating based on Figure D-2, range 0-5 A....153
Figure D-7 : IPC-2152: Current rating based on Figure D-2, range 0-2 A....153
Figure D-8 : CNES/QFT/IN.0113: Current rating [A] vs cross sectional area [mm^2] in double log scale....155
Figure D-9 : CNES/QFT/IN.0113: Track width [mm] vs cross sectional area [mm^2]....155
Figure D-10 : CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-25 A 156
Figure D-11 : CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-10 A 156
Figure D-12 : CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-5 A 157
Figure D-13 : CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-2 A 157
Figure D-14 : IPC-2221A: Current rating [A] vs cross sectional area [mm^2] in double log scale 159
Figure D-15 : IPC-2221A: Track width [mm] vs cross sectional area [mm^2]....159
Figure D-16 : IPC-2221A: Current rating based on Figure D-14, range 0-25 A 160
Figure D-17 : IPC-2221A: Current rating based on Figure D-14, range 0-10 A 160
Figure D-18 : IPC-2221A: Current rating based on Figure D-14, range 0-5 A 161
Figure D-19 : IPC-2221A: Current rating based on Figure D-14, range 0-2 A 161
Figure E-1 : PCB manufacturing tolerances for registration and annular ring for HDI PCB .162
Figure E-2 : PCB manufacturing tolerances for registration and annular ring for rigid-flex sequential PCB 163

Tables

Table 6-1: Characteristics of some example dielectric materials for laminates 32
Table 7-1: As-designed versus as-manufactured copper foil thickness 36
Table 7-2: Example of worst case as-manufactured insulation distance for laminate with double-sided copper cladding 39
Table 7-3: Tolerance on track width and spacing of internal and external layers 42
Table 7-4: Minimum as-manufactured track width and spacing for external layers as a function of copper thickness 43
Table 7-5: Minimum as-manufactured track width and spacing for internal layers as a function of copper thickness 44
Table 8-1: Minimum as-manufactured dimensions of sculptured flex conductor 59
Table 12-1: Minimum spacing and width as-designed for RF elements on external layers ... 84
Table 13-1: Legend of terms 86
Table 13-2: Current overload limits 88
Table 13-3: Minimum insulation distance as function of voltage on as-manufactured PCB for rigid laminate. 94
Table 13-4: Minimum insulation distance as function of voltage on as-manufactured PCB for flex laminate. 95
Table 13-5: Minimum double insulation distance as function of voltage on as-manufactured PCB for rigid laminate. 98
Table 13-6: Minimum double insulation distance as function of voltage on as-manufactured PCB for flex laminate. 98
Table 13-7: Minimum insulation distances on rigid PCB as function of all combined requirements (*part 1 of 4*) 102
Table 14-1: Minimum distance as-manufactured of the surface pattern to the adjacent surroundings 114
Table 14-2: Minimum distance as-manufactured of components to adjacent surroundings 116
Table 14-3: Minimum distance as-manufactured to component pads 117
Table 14-4: Minimum track length to component pads 120
Table 14-5 Legend for dimensions of components and footprint 122
Table 14-6 As-manufactured pad sizes for bipolar components 123
Table 14-7: As-manufactured pad sizes for SOIC components 124
Table 14-8: As-manufactured pad sizes for J-leaded components 125
Table 14-9: As-manufactured pad sizes for LCC components 127
Table 14-10: As-manufactured pad sizes for FP and QFP components 128
Table 14-11: As-designed pad diameter for AAD components 129

Table C-1 : Example of technical capabilities of PCB manufacturer as specified in the PID 146