DIN EN 16602-70-28:2015-06 (E)

Space product assurance - Repair and modification of printed circuit board assemblies for space use; English version EN 16602-70-28:2014

Content

page

Foreword 9

1 Scope 10

2 Normative references 11

3 Terms, definitions and abbreviated terms 12

3.1 Terms from other standards 12

3.2 Terms specific to the present standard 12

3.3 Abbreviated terms 13

4 Requirements 14

4.1 Basic requirements 14

4.1.1 Hazard, health and safety precautions 14

4.1.2 Materials 14

4.1.3 Facilities 14

4.1.4 General 14

4.2 Repairs 15

4.2.1 Repair criteria 15

4.2.2 Number of repairs 15

4.3 Modifications 15

4.3.1 Modification criteria 15

4.3.2 Number of modifications 16

4.4 Rework 16

4.4.1 Rework criteria 16

4.4.2 Number of reworks 16

4.5 Other requirements 16

4.6 Removal of conformal coating 17

4.6.1 Requirements 17

4.6.2 Procedure 17

4.6.3 Acceptance criteria 17

4.7 Solder joint removal and unclinching 18
4.7.1 Procedure 18
4.7.2 Acceptance criteria 18
4.8 Repair of damaged gold-plated areas 18
4.8.1 Requirements 18
4.8.2 Procedure 18
4.8.3 Acceptance criteria 19
4.9 Repair of damaged conductor tracks 19
4.9.1 Requirements 19
4.9.2 Procedure 19
4.9.3 Acceptance criteria 20
4.10 Repair of lifted conductors 20
4.10.1 Requirements 20
4.10.2 Procedure 20
4.10.3 Acceptance criteria 20
4.11 Repair of lifted terminal areas (pads) 21
4.11.1 Requirements 21
4.11.2 Procedure 21
4.11.3 Acceptance criteria 21
4.12 Terminal post replacement 21
4.12.1 Requirements 21
4.12.2 Procedure 21
4.12.3 Acceptance criteria 21
4.13 Wire-to-wire joints 22
4.13.1 Requirements 22
4.13.2 Procedure 22
4.13.3 Acceptance criteria 22
4.14 Addition of components 22
4.14.1 Requirements 22
4.14.2 Procedure 23
4.14.3 Acceptance criteria 23
4.15 Removal and replacement of axial and multi-lead components 24
4.15.1 Requirements 24
4.15.2 Procedure 24
4.15.3 Acceptance criteria 24
4.16 Removal and replacement of flat-pack components 24
4.16.1 Requirements 24
4.16.2 Procedure 24

4.16.3 Acceptance criteria 25
4.17 Modification of component connections 25
4.17.1 Requirements 25
4.17.2 Procedure 25
4.17.3 Acceptance criteria 26
4.18 Cutting of internal track of a multi-layer printed circuit board 26
4.18.1 Procedure 26
4.18.2 Acceptance criteria 26
4.19 Quality assurance 26
4.19.1 General 26
4.19.2 Data 26
4.19.3 Nonconformance 27
4.19.4 Calibration 27
4.19.5 Traceability 27
4.19.6 Operator and inspector training and certification 27
Annex A (informative) Removal of conformal coating 28
A.1 Introduction 28
A.2 Tools and materials 28
A.3 Methods for the removal of conformal coating 28
A.3.1 Method for the removal of polyurethane and silicone-type coating 28
A.3.2 Method for the removal of epoxy-type coating 29
Annex B (informative) Solder joint removal and unclinching 31
B.1 Introduction 31
B.2 Tools and materials 31
B.3 Methods for solder joint removal and unclinching 31
B.3.1 Method for solder extraction with continuous vacuum 31
B.3.2 Method for solder extraction using sucker 32
B.3.3 Method for hot jet extraction 33
B.3.4 Method for the use of wicking braid 33
B.3.5 Method for unclinching of leads 34
Annex C (informative) Repair of damaged gold-plated areas 35
C.1 Introduction 35
C.2 Tools and materials 35
C.3 Methods for the repair of damaged gold-plated areas 35
C.3.1 Method for the removal of solder splatter on gold plating 35
Annex D (informative) Repair of damaged conductor tracks 36
D.1 Introduction 36

D.2 Tools and materials 36
D.3 Method for the repair of damaged conductor tracks 36

Annex E (informative) Repair of lifted conductors 37

E.1 Introduction 37
E.2 Tools and materials 37
E.3 Methods for repair of lifted conductors 38
E.3.1 Method for the use of epoxy under conductor 38
E.3.2 Method for the use of epoxy over conductor 38

Annex F (informative) Repair of lifted terminal areas (pads) 39

F.1 Introduction 39
F.2 Tools and materials 40
F.3 Method for the repair of lifted terminal areas (pads) 40

Annex G (informative) Terminal post replacement 41

G.1 Introduction 41
G.2 Tools and materials 41
G.3 Method for the replacement of terminal post 41

Annex H (informative) Wire-to-wire joints 43

H.1 Introduction 43
H.2 Tools and materials 43
H.3 Method for wire-to-wire joining 43

Annex I (informative) Addition of components 45

I.1 Introduction 45
I.2 Tools and materials 45
I.3 Methods for addition of components 46
I.3.1 Method for additional components mounted on reverse (non-component) side of board 46
I.3.2 Method for additional components mounted on component side of board 47
I.3.3 Method for additional components mounted on terminal posts, including “piggyback“ mounting 48
I.3.4 Method for additional components mounted (on reverse side or on component side of board) using staking compound 49
I.3.5 Method for additional components mounted (on reverse side or on component side of board) to leads of adjacent components 50
I.3.6 Method for the addition of a wire link onto soldered chips on a single side piece of PCB with appropriate pads 55
I.3.7 Method for the addition of a wire link onto metallized cap of chips directly glued on PCB 56

Annex J (informative) Removal and replacement of axial and multi-lead components 57

J.1 Introduction 57

J.2 Tools and materials 57

J.3 Methods for removal and replacement of axial and multi-lead components 57

J.3.1 Method for the removal of components with axial leads (destructive removal) 57

J.3.2 Method for the removal of multi-lead components (destructive removal) ... 58

Annex K (informative) Removal and replacement of flat-pack components 60

K.1 Introduction 60

K.2 Tools and materials 60

K.3 Method for the removal and replacement of flat-pack components 60

Annex L (informative) Modification of component connections 62

L.1 Introduction 62

L.2 Tools and materials 62

L.3 Methods for modification of component connections 62

L.3.1 Method for the soldering of a wrap-around connection to an extended component lead 62

L.3.2 Method for the soldering of component lead to a stud lead mounted into an existing hole 63

L.3.3 Method for mounting a dual-in-line (DIL) package with or without a wire link soldered onto a cropped lead 64

L.3.4 Method for mounting a connector with or without a wire link soldered onto a cropped lead 66

L.3.5 Method for the addition of a wire link into a plated-through hole occupied by a flat-section lead 67

L.3.6 Method for the addition of a wire link on top of a flat-pack lead 69

L.3.7 Method for the isolation of a component lead 69

L.3.8 Method for the addition of a wire link onto terminal pad of soldered chips . 71

Annex M (informative) Cutting of internal track of a multi-layer printed circuit board 73

M.1 Introduction 73

M.2 Tools and materials 73

M.3 Method for cutting the internal track of a multi-layer printed circuit board 73

Bibliography 75

Figures

Figure A-1 : Removal of coating by thermal parting device 30

Figure B-1 : Continuous vacuum solder extraction on stud lead 32
Figure B-2 : Pulse-type solder sucker in use 32
Figure B-3 : Lifting individual leads with hot jet 33
Figure B-4 : Cross-sectional view of wicking method 34
Figure B-5 : Hot unclinching with thermal parting device 34
Figure E-1 : Lifted conductors 37
Figure E-2 : Repair using epoxy under conductor 38
Figure E-3 : Repair using epoxy over conductor 38
Figure F-1 : Lifted terminal area 39
Figure F-2 : Terminal areas without track 39
Figure F-3 : Terminal areas with track attached 40
Figure G-1 : Terminal post replacement 42
Figure H-1 : Use of approved type support clamp/heat sink 44
Figure I-1 : Additional components mounted on reverse (non-component) side of board 47
Figure I-2 : Additional components mounted on component side of board 48
Figure I-3 :“Piggyback” mounting of one component on top of another 49
Figure I-4 : Mounting and wiring of additional axially-leaded components mounted (on reverse side or on component side of board) using staking compound 51
Figure I-5 : Upside down mounting and wiring of additional side-brazed DIL component (on reverse side or on component side of board) using staking compound 52
Figure I-6 : Mounting of additional non-axially leaded components, e.g. capacitors, with wire connecting top or bottom sides of the circuit board using staking compound (on reverse side or on component side of board) 52
Figure I-7 : Mounting of additional component (on component side of board) with wire connections on reverse side of board using staking compound 53
Figure I-8 : Mounting of additional component (on reverse side of board) across extended leads of adjacent components 53
Figure I-9 : Mounting of additional component by linking to a “pigtailed” lead of an adjacent component 54
Figure I-10 : Mounting of additional component by linking to lead of an adjacent transistor (or other large component) 55
Figure I-11 : Addition of a wire link onto metallized cap of chips directly glued on PCB 56
Figure J-1 : Removal of multi-lead components, clipping of component leads 58
Figure J-2 : Removal of multi-lead components, removal of remaining component leads 59
Figure K-1 : Removal of flat-pack components 61
Figure L-1 : Soldering of a wrap-around connection to an extended component lead 63
Figure L-2 : Soldering of component lead to a stud lead mounted into an existing hole 64
Figure L-3 : Mounting a dual-in-line package with or without a wire link soldered onto a cropped lead (cropped lead without connection and cropped lead with connection led through hole and onto board) 65
Figure L-4 : Mounting a dual-in-line package with or without a wire link soldered onto a cropped lead (wire link passing away from board) 66

Figure L-5 : Mounting a connector with a wire link soldered onto a cropped lead 67
Figure L-6 : Addition of a wire link into a plated through hole occupied by a flat-section lead (wire link entering from the reverse side of the board) 68
Figure L-7 : Addition of a wire link into a plated through hole occupied by a flat-section lead (wire link entering from the component side of the board)..... 68
Figure L-8 : Addition of a wire link on top of a flat-pack lead..... 69
Figure L-9 : Isolation of a component lead..... 71
Figure L-10 : Addition of a wire link onto terminal pad of soldered chips 72
Figure M-1 : Cutting of internal track of a multi-layer circuit board..... 74

Tables

Table 4-1: Wire diameters for given conductor widths 19