

ISO 21806-10:2021 (E)

Road vehicles — Media Oriented Systems Transport (MOST) — Part 10: 150-Mbit/s coaxial physical layer

Contents

	Foreword
	Introduction
1	Scope
2	Normative references
3	Terms and definitions
4	Symbols and abbreviated terms
4.1	Symbols
4.2	Abbreviated terms
5	Conventions
6	Physical layer service interface to OSI data link layer
6.1	Overview
6.2	Data type definitions
6.3	Event indications and action requests
6.3.1	P_EVENT.INDICATE
6.3.2	P_ACTION.REQUEST
6.4	Parameters
6.4.1	PHY_Event
6.4.2	PHY_Request
7	Basic physical layer requirements
7.1	Logic terminology
7.1.1	Single-ended low-voltage digital signals
7.1.2	Differential LVDS signals
7.2	Specification points (SPs)
7.3	Phase variation
7.3.1	General
7.3.2	Wander
7.3.3	Jitter
7.3.4	Clock recovery and reference clock
7.3.4.1	General
7.3.4.2	Golden PLL
7.3.4.3	Jitter filter
7.3.5	Link quality
7.3.5.1	General
7.3.5.2	Alignment jitter
7.3.5.3	Transferred jitter
7.3.6	MOST network quality
7.3.6.1	Receiver tolerance
7.3.6.2	TimingMaster delay tolerance
8	MOST150 cPHY requirements
8.1	General MOST network parameters
8.1.1	MOST network coding
8.1.1.1	General
8.1.1.2	Pulse characteristics
8.1.1.3	Unit interval definition

8.1.1.4	DC balance
8.1.2	Link and interconnect type
8.1.3	SP details
8.1.4	Analogue frontend
8.1.5	Integration of coaxial transceiver
8.2	Models and measurement methods
8.2.1	Golden PLL
8.2.2	Jitter filter
8.2.3	Retimed bypass mode and stress pattern
9	Link specifications
9.1	General
9.2	SP1
9.3	SP2
9.4	Coaxial link requirements
9.4.1	Coaxial interconnect, length and attenuation
9.4.2	Characteristic impedance and return loss (LRL)
9.4.2.1	General
9.4.2.2	Coaxial interconnect, characteristic impedance and LRL
9.4.2.3	PCB interfaces, characteristic impedance and return loss
9.5	SP3
9.6	SP4
10	Power-on and power-off
10.1	Frequency reference and power supply
10.2	Power supply monitoring circuitry
10.3	Coaxial transceiver ECC and CEC
10.3.1	General
10.3.2	CTR requirements
10.3.3	ECC requirements
10.3.4	ECC power-on and power-off sequence
10.3.4.1	General
10.3.4.2	Power-on sequence example scenario
10.3.4.3	Power-off sequence example scenario
10.3.5	CEC requirements
10.3.5.1	CEC functional requirements
10.3.5.2	CEC power state requirements
10.3.6	CEC power-on and power-off sequence
10.3.6.1	General
10.3.6.2	Power-on sequence example scenario
10.3.6.3	Power-off sequence example scenario
11	MOST network requirements
11.1	SP4 receiver tolerance
11.2	TimingMaster delay tolerance
11.3	Environmental requirements and considerations
12	Electrical interfaces
12.1	LVDS
12.2	Bit rate and frequency tolerance
13	MOST150 cPHY topologies
13.1	Daisy chain topologies
13.2	Daisy chain structure
13.3	2-port nodes
13.4	Port1 delay drift
14	Device connectors
15	SPs for cable extensions
16	Coaxial interconnect attenuation