

ISO 16845-1:2016-11 (E)

Road vehicles - Controller area network (CAN) conformance test plan - Part 1: Data link layer and physical signalling

Contents		Page
Foreword		vii
Introduction		viii
1 Scope		1
2 Normative references		1
3 Terms and definitions		1
4 Abbreviated terms		3
5 Global overview		4
5.1 Scope of test plan.....		4
5.2 Architecture of test plan.....		4
5.3 Organization.....		5
5.3.1 General organization.....		5
5.3.2 Test case organization.....		6
5.3.3 Hierarchical structure of tests.....		7
6 LT parameters		8
6.1 Overview.....		8
6.2 Description of parameters.....		8
6.2.1 Communication parameters.....		8
6.2.2 Application parameters.....		9
6.2.3 Bit rate configuration parameter variation for bit timing tests.....		10
7 Test type 1, received frame		10
7.1 Test class 1, valid frame format.....		10
7.1.1 Identifier and number of data test in base format.....		10
7.1.2 Identifier and number of data test in extended format.....		11
7.1.3 Reception after arbitration lost.....		12
7.1.4 Acceptance of non-nominal bit in base format frame.....		13
7.1.5 Acceptance of non-nominal bit in extended format frame.....		13
7.1.6 Protocol exception behaviour on non-nominal bit.....		14
7.1.7 Minimum time for bus idle after protocol exception handling.....		15
7.1.8 DLC greater than 8.....		15
7.1.9 Absent bus idle — Valid frame reception.....		16
7.1.10 Stuff acceptance test in base format frame.....		16
7.1.11 Stuff acceptance test in extended format frame.....		17
7.1.12 Message validation.....		18
7.2 Test class 2, error detection.....		19
7.2.1 Bit error in data frame.....		19
7.2.2 Stuff error for basic frame.....		19
7.2.3 Stuff error for extended frame.....		20
7.2.4 Stuff error for FD frame payload bytes.....		21
7.2.5 CRC error.....		22
7.2.6 Combination of CRC error and form error.....		23
7.2.7 Form error in data frame at “CRC delimiter” bit position.....		24
7.2.8 Form error at fixed stuff bit in FD frames.....		24
7.2.9 Form error in data frame at “ACK delimiter” bit position.....		25
7.2.10 Form error in data frame at “EOF”.....		25
7.2.11 Message non-validation.....		26
7.3 Test class 3, error frame management.....		26
7.3.1 Error flag longer than 6 bits.....		26
7.3.2 Data frame starting on the third bit of intermission field.....		27
7.3.3 Bit error in error flag.....		27
7.3.4 Form error in error delimiter.....		28

7.4	Test class 4, overload frame management.....	28
7.4.1	MAC overload generation during intermission field.....	28
7.4.2	Last bit of EOF.....	29
7.4.3	Eighth bit of an error and overload delimiter.....	29
7.4.4	Bit error in overload flag.....	30
7.4.5	Form error in overload delimiter.....	30
7.4.6	MAC overload generation during intermission field following an error frame.....	31
7.4.7	MAC overload generation during intermission field following an overload frame.....	31
7.5	Test class 5, passive error state class.....	32
7.5.1	Passive error flag completion test 1.....	32
7.5.2	Data frame acceptance after passive error frame transmission.....	33
7.5.3	Acceptance of 7 consecutive dominant bits after passive error flag.....	33
7.5.4	Passive state unchanged on further errors.....	34
7.5.5	Passive error flag completion — Test case 2.....	34
7.5.6	Form error in passive error delimiter.....	35
7.5.7	Transition from active to passive ERROR FLAG.....	35
7.6	Test class 6, error counter management.....	36
7.6.1	REC increment on bit error in active error flag.....	36
7.6.2	REC increment on bit error in overload flag.....	37
7.6.3	REC increment when active error flag is longer than 13 bits.....	37
7.6.4	REC increment when overload flag is longer than 13 bits.....	38
7.6.5	REC increment on bit error in the ACK field.....	38
7.6.6	REC increment on form error in CRC delimiter.....	38
7.6.7	REC increment on form error in ACK delimiter.....	39
7.6.8	REC increment on form error in EOF field.....	39
7.6.9	REC increment on stuff error.....	40
7.6.10	REC increment on CRC error.....	41
7.6.11	REC increment on dominant bit after end of error flag.....	41
7.6.12	REC increment on form error in error delimiter.....	42
7.6.13	REC increment on form error in overload delimiter.....	42
7.6.14	REC decrement on valid frame reception.....	43
7.6.15	REC decrement on valid frame reception during passive state.....	43
7.6.16	REC non-increment on last bit of EOF field.....	44
7.6.17	REC non-increment on 13-bit length overload flag.....	44
7.6.18	REC non-increment on 13-bit length error flag.....	45
7.6.19	REC non-increment on last bit of error delimiter.....	45
7.6.20	REC non-increment on last bit of overload delimiter.....	46
7.6.21	REC non-decrement on transmission.....	46
7.6.22	REC increment on form error at fixed stuff bit in FD frames.....	47
7.6.23	REC non-increment on protocol exception in FD frames.....	47
7.7	Test class 7, bit timing Classical CAN frame format.....	48
7.7.1	Sample point test.....	48
7.7.2	Hard synchronization on SOF reception.....	49
7.7.3	Synchronization when $e > 0$ and $e \leq \text{SJW}(N)$	49
7.7.4	Synchronization when $e > 0$ and $e > \text{SJW}(N)$	50
7.7.5	Synchronization when $e < 0$ and $ e \leq \text{SJW}(N)$	50
7.7.6	Synchronization when $e < 0$ and $ e > \text{SJW}(N)$	51
7.7.7	Glitch filtering test on positive phase error.....	51
7.7.8	Glitch filtering test on negative phase error.....	52
7.7.9	Glitch filtering test in idle state.....	53
7.7.10	Non-Synchronization after a dominant sampled bit.....	54
7.7.11	Synchronization when $e < 0$ and $ e \leq \text{SJW}(N)$ at “ACK” bit position.....	55
7.8	Test class 8, bit timing CAN FD frame format.....	55
7.8.1	Sample point test.....	55
7.8.2	Hard synchronization on “res” bit.....	58
7.8.3	Synchronization when $e > 0$ and $e \leq \text{SJW}(D)$	59
7.8.4	Synchronization when $e > 0$ and $e > \text{SJW}(D)$	61
7.8.5	Synchronization when $e < 0$ and $ e \leq \text{SJW}$	63
7.8.6	Synchronization when $e < 0$ and $ e > \text{SJW}$	65

	7.8.7	Glitch filtering test on positive phase error.....	67
	7.8.8	Glitch filtering test on negative phase error.....	69
	7.8.9	No synchronization after a dominant sampled bit.....	71
8		Test type 2, transmitted frame.....	73
	8.1	Test class 1, valid frame format.....	73
	8.1.1	Identifier and number of data bytes test in base format.....	73
	8.1.2	Identifier and number of data bytes test in extended format.....	73
	8.1.3	Arbitration in base format frame.....	74
	8.1.4	Arbitration in extended format frame test.....	75
	8.1.5	Message validation.....	76
	8.1.6	Stuff bit generation capability in base format frame.....	76
	8.1.7	Stuff bit generation capability in extended frame.....	77
	8.1.8	Transmission on the third bit of intermission field after arbitration lost.....	78
	8.2	Test class 2, error detection.....	79
	8.2.1	Bit error test in base format frame.....	79
	8.2.2	Bit error in extended format frame.....	80
	8.2.3	Stuff error test in base format frame.....	81
	8.2.4	Stuff error test in extended frame format.....	81
	8.2.5	Form error test.....	82
	8.2.6	Acknowledgement error.....	83
	8.2.7	Form field tolerance test for FD frame format.....	84
	8.2.8	Bit error at stuff bit position for FD frame payload bytes.....	84
	8.3	Test class 3, error frame management.....	85
	8.3.1	Error flag longer than 6 bit.....	85
	8.3.2	Transmission on the third bit of intermission field after error frame.....	85
	8.3.3	Bit error in error flag.....	86
	8.3.4	Form error in error delimiter.....	86
	8.4	Test class 4, overload frame management.....	87
	8.4.1	MAC overload generation in intermission field.....	87
	8.4.2	Eighth bit of an error and overload delimiter.....	88
	8.4.3	Transmission on the third bit of intermission after overload frame.....	88
	8.4.4	Bit error in overload flag.....	89
	8.4.5	Form error in overload delimiter.....	89
	8.5	Test class 5, passive error state and bus-off.....	90
	8.5.1	Acceptance of active error flag overwriting passive error flag.....	90
	8.5.2	Frame acceptance after passive error frame transmission.....	90
	8.5.3	Acceptance of 7 consecutive dominant bits after passive error flag.....	91
	8.5.4	Reception of a frame during suspend transmission.....	92
	8.5.5	Transmission of a frame after suspend transmission — Test case 1.....	92
	8.5.6	Transmission of a frame after suspend transmission — Test case 2.....	93
	8.5.7	Transmission of a frame after suspend transmission — Test case 3.....	93
	8.5.8	Transmission of a frame without suspend transmission.....	93
	8.5.9	No transmission of a frame between the third bit of intermission field and eighth bit of suspend transmission.....	94
	8.5.10	Bus-off state.....	94
	8.5.11	Bus-off recovery.....	95
	8.5.12	Completion condition for a passive error flag.....	96
	8.5.13	Form error in passive error delimiter.....	96
	8.5.14	Maximum recovery time after a corrupted frame.....	97
	8.5.15	Transition from active to passive ERROR FLAG.....	97
	8.6	Test class 6, error counter management.....	98
	8.6.1	TEC increment on bit error during active error flag.....	98
	8.6.2	TEC increment on bit error during overload flag.....	99
	8.6.3	TEC increment when active error flag is followed by dominant bits.....	99
	8.6.4	TEC increment when passive error flag is followed by dominant bits.....	100
	8.6.5	TEC increment when overload flag is followed by dominant bits.....	100
	8.6.6	TEC increment on bit error in data frame.....	101
	8.6.7	TEC increment on form error in a frame.....	102

8.6.8	TEC increment on acknowledgement error.....	102
8.6.9	TEC increment on form error in error delimiter.....	103
8.6.10	TEC increment on form error in overload delimiter.....	103
8.6.11	TEC decrement on successful frame transmission for TEC < 128.....	104
8.6.12	TEC decrement on successful frame transmission for TEC > 127.....	104
8.6.13	TEC non-increment on 13-bit long overload flag.....	105
8.6.14	TEC non-increment on 13-bit long error flag.....	105
8.6.15	TEC non-increment on form error at last bit of overload delimiter.....	106
8.6.16	TEC non-increment on form error at last bit of error delimiter.....	106
8.6.17	TEC non-increment on acknowledgement error in passive state.....	107
8.6.18	TEC increment after acknowledgement error in passive state.....	107
8.6.19	TEC non-increment on stuff error during arbitration.....	108
8.6.20	TEC non-decrement on transmission while arbitration lost.....	108
8.6.21	TEC non-increment after arbitration lost and error.....	109
8.7	Test class 7, bit timing.....	109
8.7.1	Sample point test.....	109
8.7.2	Hard synchronization on SOF reception before sample point.....	110
8.7.3	Hard synchronization on SOF reception after sample point.....	111
8.7.4	Synchronization when $e < 0$ and $ e \leq \text{SJW}(N)$	111
8.7.5	Synchronization for $e < 0$ and $ e > \text{SJW}(N)$	112
8.7.6	Glitch filtering test on negative phase error.....	113
8.7.7	Non-synchronization on dominant bit transmission.....	113
8.7.8	Synchronization before information processing time.....	114
8.7.9	Synchronization after sample point while sending a dominant bit.....	114
8.8	Test class 8, bit timing CAN FD frame format.....	115
8.8.1	Sample point test.....	115
8.8.2	Secondary sample point test.....	118
8.8.3	No synchronization within data phase bits when $e < 0$; $ e \leq \text{SJW}(D)$	121
8.8.4	Glitch filtering test on negative phase error within FD frame bits.....	123
8.8.5	No synchronization on dominant bit transmission in FD frames.....	124
9	Test type 3, bi-directional frame.....	125
9.1	Test class 1, valid frame format.....	125
9.2	Test class 2, error detection.....	125
9.3	Test class 3, active error frame management.....	125
9.4	Test class 4, overload frame management.....	125
9.5	Test class 5, passive-error state and bus-off.....	125
9.6	Test class 6, error counter management.....	126
9.6.1	REC unaffected when increasing TEC.....	126
9.6.2	TEC unaffected when increasing REC.....	126