

ISO/IEC 24739-3:2010-03 (E)

Information technology – AT attachment with packet interface-7 – Part 3: Serial transport protocols and physical interconnect (ATA/ATAPI-7 V3)

CONTENTS

FOREWORD.....	12
INTRODUCTION.....	13
1 Scope.....	14
2 Normative references	14
3 Terms and definitions, abbreviations and conventions	14
3.1 Terms and definitions	14
3.2 Abbreviations	21
3.3 Conventions	22
3.3.1 General	22
3.3.2 Precedence	22
3.3.3 Lists	23
3.3.4 Keywords	23
3.3.5 Numbering.....	24
3.3.6 Signal conventions	24
3.3.7 Bit conventions	24
3.3.8 State diagram conventions	24
3.3.9 Timing conventions.....	25
3.3.10 Byte ordering for data transfers	26
4 General operational requirements.....	28
5 I/O register descriptions	28
6 Command descriptions	28
7 Parallel interface physical and electrical requirements.....	28
8 Parallel interface signal assignments and descriptions	28
9 Parallel interface general operating requirements of the physical, data link, and transport layers	28
10 Parallel interface register addressing.....	28
11 Parallel interface transport protocols	29
12 Parallel interface timing.....	29
13 Serial interface general overview.....	29
13.1 Overview	29
13.2 Sub-module operation	30
13.3 Parallel ATA emulation	31
13.3.1 General	31
13.3.2 Software reset	32
13.3.3 Device 0-only emulation	32
13.3.4 Device 0/Device 1 emulation (optional).....	33
14 Serial interface physical layer.....	34
14.1 Overview	34
14.1.1 General	34
14.1.2 List of services	34
14.2 Connectors specifications.....	35
14.2.1 Overview	35
14.2.2 General descriptions.....	35
14.2.3 Connector drawings.....	37
14.2.4 Connector pinouts	44

14.2.5	Backplane connector configuration and blind-mating tolerance	45
14.2.6	Connector locations	45
14.2.7	Connector conformance requirements	49
14.3	Cable assemblies	55
14.4	Phy (physical layer electronics)	56
14.4.1	Physical plant as a system	56
14.4.2	Bit error rate testing	60
14.4.3	Frame error rate testing.....	61
14.4.4	Test requirements, non-compliant patterns	62
14.4.5	Test requirements, compliant frame patterns	62
14.4.6	Test requirements, loopback	62
14.4.7	Test Method for Data Rate Frequency Variation, SSC Profile	63
14.4.8	Block diagram	63
14.4.9	Electrical specifications	65
14.4.10	Frame error-rate measurements	68
14.4.11	Receiver Differential voltage	68
14.4.12	Receiver Common-mode voltage	68
14.4.13	Transmitter Differential voltage.....	68
14.4.14	Transmitter Common-mode voltage	68
14.4.15	Rise/fall times	68
14.5	Electrical features	69
14.5.1	Definitions	69
14.5.2	Differential voltage/timing (EYE) diagram	70
14.5.3	Spread spectrum clocking (SSC)	73
14.5.4	Common-mode biasing	75
14.5.5	Matching	75
14.5.6	Out of band signalling.....	76
14.6	Elasticity buffer management	94
14.7	BIST (Built in self test)	94
14.7.1	General	94
14.7.2	Loopback testing	94
15	Serial interface Link layer	97
15.1	Overview	97
15.1.1	General	97
15.1.2	Frame transmission	97
15.1.3	Frame receipt	97
15.2	Encoding method	98
15.2.1	General	98
15.2.2	Notation and conventions	98
15.2.3	Character code	99
15.2.4	Transmission summary.....	106
15.2.5	Reception.....	107
15.3	Transmission method	108
15.4	Primitives	109
15.4.1	Overview.....	109
15.4.2	Primitive descriptions	110
15.4.3	Primitive encoding.....	111
15.4.4	ALIGN primitive	111
15.4.5	CONT primitive.....	112

15.4.6	DMAT primitive.....	113
15.4.7	EOF primitive	114
15.4.8	HOLD/HOLDA primitives	114
15.4.9	PMREQ_P, PMREQ_S, PMACK, and PMNAK primitives	116
15.4.10	R_ERR primitive.....	116
15.4.11	R_IP primitive.....	116
15.4.12	R_OK primitive	116
15.4.13	R_RDY primitive.....	116
15.4.14	SOF primitive	116
15.4.15	SYNC primitive.....	116
15.4.16	WTRM primitive.....	116
15.4.17	X_RDY primitive.....	116
15.4.18	Examples	116
15.5	CRC calculation	120
15.6	Scrambling	121
15.6.1	Frame content scrambling	121
15.6.2	Repeated primitive suppression.....	121
15.6.3	Link layer state diagrams.....	121
	Serial interface Transport layer.....	139
16.1	Transport layer overview	139
16.1.1	General	139
16.1.2	FIS construction	139
16.1.3	FIS decomposition.....	139
16.2	Frame Information Structure (FIS).....	139
16.2.1	Overview.....	139
16.2.2	Payload content	139
16.2.3	FIS types.....	140
16.2.4	Register, Device to Host.....	141
16.2.5	Set Device Bits - Device to Host.....	143
16.2.6	DMA Activate, Device to Host.....	144
16.2.7	First Party DMA Setup, Device to Host or Host to Device (bidirectional)	145
16.2.8	BIST Activate, bidirectional	146
16.2.9	PIO Setup, Device to Host.....	148
16.2.10	Data, Host to Device or Device to Host (bidirectional)	150
16.3	Host transport states	151
16.3.1	Host transport idle state diagram.....	151
16.3.2	Host Transport transmit command FIS diagram.....	153
16.3.3	Host Transport transmit control FIS diagram	154
16.3.4	Host Transport transmit First Party DMA Setup, Device to Host or Host to Device FIS state diagram	155
16.3.5	Host Transport transmit BIST Activate FIS	156
16.3.6	Host Transport decompose Register FIS diagram.....	157
16.3.7	Host Transport decompose a Set Device Bits FIS state diagram	158
16.3.8	Host Transport decompose a DMA Activate FIS diagram and DMA Data Transfer	158
16.3.9	Host Transport decompose a PIO Setup FIS state diagram	161
16.3.10	Host Transport decompose a First Party DMA Setup FIS state diagram.....	164
16.3.11	Host transport decompose a BIST Activate FIS state diagram	165

16.4	Device transport states	167
16.4.1	Device transport idle state diagram	167
16.4.2	Device Transport send Register, Device to Host state diagram	168
16.4.3	Device Transport send Set Device Bits FIS state diagram	169
16.4.4	Device Transport transmit PIO Setup, Device to Host FIS state diagram	170
16.4.5	Device Transport transmit DMA Activate FIS state diagram	170
16.4.6	Device Transport transmit First Party DMA Setup, Device to Host FIS state diagram	171
16.4.7	Device Transport transmit Data, Device to Host FIS diagram	172
16.4.8	Device Transport transmit BIST Activate FIS diagram	174
16.4.9	Device Transport decompose Register, Host to Device state diagram	176
16.4.10	Device Transport decompose Data (Host to Device) FIS state diagram	177
16.4.11	Device Transport decompose First Party DMA Setup FIS, Host to Device or Device to Host state diagram	178
16.4.12	Device Transport decompose a BIST Activate FIS state diagram	179
17	Serial interface Device Command Layer Protocol	180
17.1	COMRESET or SRST sent by Host	180
17.2	Power-on and COMRESET protocol diagram	180
17.3	Device Idle protocol	182
17.4	Software reset protocol	185
17.5	EXECUTE DEVICE DIAGNOSTIC command protocol	187
17.6	DEVICE RESET command protocol	188
17.7	Non-data command protocol	188
17.8	PIO data-in command protocol	189
17.9	PIO data-out command protocol	190
17.10	DMA data-in command protocol	192
17.11	DMA data out command protocol	193
17.12	PACKET protocol	195
17.13	READ DMA QUEUED command protocol	200
17.14	WRITE DMA QUEUED command protocol	201
18	Host command layer state diagram	204
18.1	Overview	204
18.2	Device Emulation of nIEN with Interrupt Pending	207
19	Serial interface host adapter register interface	208
19.1	Overview	208
19.2	SStatus, SError and SControl registers	209
19.2.1	General	209
19.2.2	SStatus register	209
19.2.3	SErrror register	210
19.2.4	SControl register	211
20	Serial interface error handling	212
20.1	Architecture	212
20.2	Phy error handling overview	213
20.2.1	Error detection	213
20.2.2	Error control actions	214
20.2.3	Error reporting	214

20.3	Link error handling overview.....	214
20.3.1	Error detection.....	214
20.3.2	Error control actions	215
20.3.3	Error reporting	216
20.4	Transport error handling	216
20.4.1	Overview	216
20.4.2	Error detection.....	216
20.4.3	Error control actions	217
20.4.4	Error reporting	218
20.5	Software error handling overview	218
20.5.1	General	218
20.5.2	Error detection.....	218
20.5.3	Error control actions	219
Annex A (informative)	Command Set summary	220
Annex B (informative)	Design and programming considerations for large physical sector devices.....	220
Annex C (informative)	Device determination of cable type.....	220
Annex D (informative)	Signal integrity and UDMA guide.....	220
Annex E (informative)	Register selection address summary	220
Annex F (informative)	SAMPLE code for Serial CRC Scrambling	221
F.1	CRC calculation.....	221
F.1.1	Overview	221
F.1.2	Maximum frame size	221
F.1.3	Example code for CRC algorithm.....	221
F.1.4	Example CRC implementation output	224
F.2	Scrambling calculation.....	224
F.2.1	Overview	224
F.2.2	Example code for scrambling algorithm	224
F.2.3	Example scrambler implementation	227
F.3	Example frame	228
Annex G (informative)	FIS Type field value selection	229
G.1	Overview	229
G.2	Type field values	229
Annex H (informative)	Physical Layer implementation examples	230
H.1	Cable construction example.....	230
H.2	Contact material and plating	231
H.3	Relationship of frequency to the jitter specification	231
H.4	Sampling BER and jitter formulas	232
H.5	DC and AC coupled transmitter examples.....	233
H.6	OOB signal and squelch detector examples.....	235
Annex I (informative)	Command Processing example.....	238
I.1	Non-data commands.....	238
I.1.1	General.....	238
I.1.2	Legacy DMA read by host from device.....	238
I.1.3	Legacy DMA write by host to device	238
I.1.4	PIO data read from the device	239

I.1.5	PIO data write to the device	239
I.1.6	READ DMA QUEUED example	240
I.1.7	WRITE DMA QUEUED example	241
I.1.8	ATAPI PACKET commands with PIO data-in	241
I.1.9	ATAPI PACKET commands with PIO data out	242
I.1.10	ATAPI PACKET commands with DMA data-in	243
I.1.11	ATAPI PACKET commands with DMA data-out	244
I.1.12	First Party DMA read of host memory by device	245
I.1.13	First Party DMA write of host memory by device	245
I.2	Odd word count considerations	245
I.2.1	General	245
I.2.2	Legacy DMA read from target for odd word count	246
I.2.3	Legacy DMA write by host to target for odd word count	246
I.2.4	PIO data read from the device	246
I.2.5	PIO data write to the device	247
I.2.6	First Party DMA read of host memory by device	247
I.2.7	First Party DMA write of host memory by device	247
	Bibliography	249
	Figure 1 – ATA document relationships	13
	Figure 2 – State diagram convention	25
	Figure 3 – Byte, word and DWORD relationships	28
	Figure 4 – Standard ATA device connectivity	29
	Figure 5 – The serial implementation of ATA connectivity	30
	Figure 6 – Communication layers	31
	Figure 7 – Serial implementation connector examples	36
	Figure 8 – Device plug connector part 1 of 2	37
	Figure 9 – Device plug connector part 2 of 2	38
	Figure 10 – Non-Latching Signal Cable receptacle connector interface dimensions	39
	Figure 11 – Optional Latching Signal Cable Receptacle connector interface dimensions	40
	Figure 12 – Host plug connector interface dimension	41
	Figure 13 – Host receptacle connector interface dimensions	42
	Figure 14 – Non-Latching Power cable receptacle connector interface dimensions	43
	Figure 15 – Optional Latching Power Cable Receptacle	43
	Figure 16 – Connector pair blind-mate misalignment tolerance	45
	Figure 17 – Device-backplane mating configuration	45
	Figure 18 – Device plug connector location on 95 mm (3.5”) device	46
	Figure 19 – Device plug connector location on 65 mm (2.5”) device	47
	Figure 20 – Recommended host plug spacing for Non-Latching Connectors	48
	Figure 21 – Recommended host plug connector clearance and Orientation for Optional Latching Connectors	49
	Figure 22 – Signals and grounds assigned in direct connect and cabled	56
	Figure 23 – Low transition density pattern	58
	Figure 24 – Half-rate / quarter-rate high transition density pattern	58
	Figure 25 – Low-frequency spectral content pattern	59
	Figure 26 – Simultaneous switching outputs patterns	59

Figure 27 – Composite patterns	60
Figure 28 – Compliant test patterns	62
Figure 29 – Physical plant overall block diagram.....	64
Figure 30 – Signal rise and fall times	68
Figure 31 – Transmit test fixture	69
Figure 32 – Receive test fixture	69
Figure 33 – Voltage / timing margin base diagram	70
Figure 34 – Jitter output/tolerance mask	71
Figure 35 – Jitter measurement example	73
Figure 36 – Triangular frequency modulation profile.....	74
Figure 37 – Spectral fundamental frequency comparison	74
Figure 38 – Out of band signals	76
Figure 39 – Host phy initialization state machine (States HP1-HP13).....	78
Figure 40 – Device phy initialization state machine (States DP1-DP12)	83
Figure 41 – COMRESET sequence	87
Figure 42 – COMINIT sequence.....	89
Figure 43 – Power-on sequence	91
Figure 44 – ON to Partial/Slumber, host initiated	92
Figure 45 – ON to Partial/Slumber, device initiated	93
Figure 46 – Loopback, far-end retimed.....	95
Figure 47 – Loopback, far-end analog.....	96
Figure 48 – Loopback, near-end analog	97
Figure 49 – Bit designations	98
Figure 50 – Nomenclature reference	99
Figure 51 – Conversion examples	99
Figure 52 – Coding examples	102
Figure 53 – Bit ordering and significance	107
Figure 54 – Single bit error with two character delay.....	108
Figure 55 – Single bit error with one character delay	108
Figure 56 – Transmission structures	109
Figure 57 – CONT usage example	117
Figure 58 – Link idle state diagram (States L1, LS1-LS3).....	122
Figure 59 – Link transmit state diagram (States LT1-LT9).....	125
Figure 60 – Link receive state diagram (States LR1-LR9)	131
Figure 61 – Link power mode state diagram (States LPM1-LPM8)	136
Figure 62 – Register, Host to Device FIS layout.....	140
Figure 63 – Register, Device to Host FIS layout.....	141
Figure 64 – Set Device Bit, Device to Host FIS layout.....	143
Figure 65 – DMA Activate, Device to Host FIS layout.....	144
Figure 66 – First Party DMA Setup – Device to Host FIS layout	145
Figure 67 – BIST Activate, Bidirectional	146
Figure 68 – PIO Setup, Device to Host FIS layout.....	148
Figure 69 – Data, Host to Device or Device to Host FIS layout.....	150

Figure 70 – Host transport idle state diagram (States HTI1-HTI2)	151
Figure 71 – Host transport transmit command FIS diagram (States HTCM1-HTCM2)	153
Figure 72 – Host transport transmit control FIS diagram (States HTCR1-HTCR2)	154
Figure 73 – Host transport transmit First Party DMA setup – Device to host or host to device FIS (States HTDMASTERUP0-HTDMASTERUP1)	155
Figure 74 – Host transport transmit BIST activate FIS (States HTXBIST0-HTXBIST1)	156
Figure 75 – Host transport decompose register FIS diagram (States HTR1- HTR2).....	157
Figure 76 – Host transport decompose Set Device Bits FIS state diagram (States HTDB0-HTDB1)	158
Figure 77 – Host transport decompose DMA activate FIS diagram (States HTDA1-HTDA5)	159
Figure 78 – Host transport decompose PIO setup FIS state diagram (States HTPS1-HTPS6).....	162
Figure 79 – Host transport decompose First Party DMA Setup FIS state diagram (State HTDS1)	165
Figure 80 – Host transport decompose BIST activate FIS state diagram (State HTRBIST0-HTRBIST1)	166
Figure 81 – Device transport idle state diagram (States DTI0-DTI1).....	167
Figure 82 – Device transport send register – Device to host state diagram (DTR0-DTR1).....	168
Figure 83 – Device transport send set device bits FIS state diagram (DTDB0-DTDB1).....	169
Figure 84 – Device transport transmit PIO setup – Device to Host FIS state diagram (States DTPIOSTUP0-DTPIOSTUP1).....	170
Figure 85 – Device transport transmit DMA activate FIS state diagram (States DTDMAACT0-DTDMAACT1)	171
Figure 86 – Device transport transmit First Party DMA setup – Device to Host state diagram (States DTDMASTERUP0-DTDMASTERUP1).....	172
Figure 87 – Device transport transmit data – Device to Host FIS diagram (State DTDATAI0-DTDATAI2)	173
Figure 88 – Device transport transmit BIST activate FIS diagram (States DTXBIST0-DTXBIST1)	175
Figure 89 – Device transport decompose register – Host to Device state diagram (State DTCMD0)	176
Figure 90 – Device transport decompose data (host to device) FIS state diagram (States DTDATAO0-DTDATAO2)	177
Figure 91 – Device transport decompose First Party DMA Setup FIS – Host to Device or device to host state diagram (State DTDMASTERUP0)	178
Figure 92 – Device transport decompose BIST activate FIS (States DTRBIST0-DTRBIST1)	179
Figure 93 – Power on and COMRESET protocol (States DHR0-DHR3)	180
Figure 94 – Device idle protocol (States DI0-DI7)	182
Figure 95 – Software reset protocol (States DSR0-DSR3).....	185
Figure 96 – EXECUTE DEVICE DIAGNOSTIC command protocol (States DEDD0-DEDD2)	187
Figure 97 – DEVICE RESET command protocol (States DDR0-DDR1).....	188
Figure 98 – Non-data command protocol (States DND0-DND1).....	188
Figure 99 – PIO data-in command protocol (States DPPIOI0-DPPIOI3)	189
Figure 100 – PIO data-out command protocol (States DPPIOO0-DPPIOO3).....	190

Figure 101 – DMA data-in command protocol (States DDMAI0-DDMAI1)	192
Figure 102 – DMA data-out command protocol (States DDMAO0-DDMAO3)	193
Figure 103 – PACKET command protocol (States DP0-DP16).....	195
Figure 104 – READ DMA QUEUED command protocol (States DDMAQI0-DDMAQI4).....	200
Figure 105 – WRITE DMA QUEUED command protocol (DDMAOQ0-DDMAOQ5).....	202
Figure 106 – Host adapter state diagram (States HA0-HA2).....	204
Figure 107 – Error handling architecture	212
Figure H.1 – Cable construction example.....	230
Figure H.2 – Jitter as a function of frequency	232
Figure H.3 – Sampling bit error rate formulae	233
Figure H.4 – Transmitter example 1	234
Figure H.5 – Transmitter example 2	235
Figure H.6 – OOB signal detector	236
Figure H.7 – Squelch detector	237
Table 1 – PACKET delivered command sets	13
Table 2 – 16-bit Transfer Byte order	27
Table 3 – 8-bit Transfer Byte order	27
Table 4 – Device plug connector pin definition	44
Table 5 – Signal integrity requirements and test procedures	50
Table 6 – Housing and contact electrical parameters, test procedures and requirements.....	52
Table 7 – Mechanical test procedures and requirements.....	53
Table 8 – Environmental parameters, test procedures, and requirements.....	54
Table 9 – Additional requirement	54
Table 10 – Connector test sequences	55
Table 11 – Physical Layer Electrical Requirements	66
Table 12 – Voltage / timing margin definition	71
Table 13 – Sampling differential noise budget.....	72
Table 14 – Desired peak amplitude reduction by SSC.....	75
Table 15 – Out of band signal times.....	76
Table 16 – Interface power states	90
Table 17 – 5b/6b coding	101
Table 18 – 3b/4b coding	101
Table 19 – Valid data characters.....	103
Table 20 – Valid control characters.....	106
Table 21 – Description of primitives	110
Table 22 – Primitive encoding.....	111
Table 23 – Valid CONT Transmission Sequences	112
Table 24 – Latency example	115
Table 25 – SRST write from host to device transmission breaking through a device to host Data FIS.....	115
Table 26 – Shadow Command Block and Shadow Control Block transmission example	118

Table 27 – Data from host to device transmission example	119
Table 28 – DMA data from host to device, device terminates transmission example.....	120
Table 29 – SCR definition	209
Table 30 – SCR definition	209
Table F.1 – CRC and scrambler calculation example - PIO Write Command	228
Table G.1 – Type field values	229
Table H.1 – Contact material and plating example	231