

# ISO/IEC 13213:1994-10 (E)

## Information technology - Microprocessor systems - Control and Status Registers (CSR) architecture for microcomputer buses

---

### Contents

Page

1.	Document structure and notation.....	1
1.1	Document structure .....	1
1.2	References .....	1
1.3	Conformance levels .....	1
1.4	Technical glossary .....	2
1.5	Bit, byte, and quadlet ordering .....	9
1.6	Numerical values .....	9
1.7	C code notation .....	10
1.8	CSR, ROM, and field notation .....	10
1.9	Register specification format.....	11
1.10	Reserved registers and fields .....	12
2.	Objectives and scope .....	15
2.1	Scope.....	15
2.2	Objectives .....	15
3.	Transaction set requirements .....	17
3.1	Transaction overview.....	17
3.2	Read and write transactions .....	17
3.3	Noncoherent lock transactions 1.....	8
3.4	Transaction errors.....	20
3.5	Immediate effects .....	21
4.	Node addressing .....	23
4.1	Node addresses.....	23
4.2	Extended addressing .....	23
4.3	64-bit fixed addressing .....	25
4.4	Private addresses.....	26
4.5	Initial node space .....	26
4.6	Extended address spaces .....	27
4.7	Indirect space .....	28
4.8	Address space offsets.....	29
5.	Node architectures.....	31
5.1	Modules, nodes, and units .....	31
5.2	Node states .....	32
5.3	Node testing.....	33
5.3.1	Access-path tests.....	33
5.3.2	Reset test .....	33
5.3.3	Diagnostic tests.....	34
5.3.4	Non-standard diagnostic tests.....	35
5.4	Multinode modules.....	36
5.5	On-line replacement (OLR).....	36
6.	Unit architectures .....	39
6.2	Interrupts .....	39
6.2.1	Interrupt-target registers .....	39
6.2.2	Interrupt-poll registers.....	40
6.3	Message passing.....	41
6.4	Globally synchronized clocks.....	41
6.4.1	Clock overview .....	41
6.4.2	Clock synchronization .....	42
6.4.3	Clock update models .....	43
6.4.4	Updating clock registers .....	44
6.4.5	Clock accuracy requirements .....	45
6.5	Memory unit architectures .....	45
6.6	Unit architecture environment .....	45

7.	CSR definitions .....	47
7.	1 Register names and offsets .....	47
7.2	Minimal implementations .....	50
7.3	Unsupported register accesses .....	51
7.4	Register definitions .....	51
7.4.1	STATE_CLEAR .....	51
7.4.2	STATE_SET .....	54
7.4.3	NODE_JDS .....	55
7.4.4	RESET_START .....	56
7.4.5	INDIRECT_ADDRESS .....	57
7.4.6	INDIRECT_DATA .....	58
7.4.7	SPLIT_TIMEOUT .....	58
7.4.8	ARGUMENT .....	59
7.4.9	TEST_START .....	61
7.4.10	TEST_STATUS .....	64
7.4.11	UNITS_BASE .....	66
7.4.12	UNITS_BOUND .....	68
7.4.13	MEMORY_BASE .....	69
7.4.14	MEMORY_BOUND .....	70
7.4.15	INTERRUPT_TARGET .....	71
7.4.16	INTERRUPT_MASK .....	72
7.4.17	CLOCK_VALUE .....	72
7.4.18	CLOCK_TICK_PERIOD .....	74
7.4.19	CLOCK_STROBE_ARRIVED .....	75
7.4.20	CLOCK_STROBE_INFO .....	76
7.4.21	Message targets .....	76
7.4.22	ERROR_LOG registers .....	77
8.	ROM specification .....	79
8.1	Introduction .....	79
8.1.1	ROM design assumptions .....	79
8.1.2	ROM formats .....	79
8.1.3	Driver and diagnostic identifiers .....	79
8.1.4	ASCII text .....	81
8.1.5	CRC calculations .....	81
8.2	ROM formats .....	83
8.2.1	First ROM quadlet .....	83
8.2.2	Minimal ROM format .....	83
8.2.3	General ROM format .....	83
8.2.4	Directory formats .....	84
8.2.5	Leaf format .....	86
8.2.6	Textual_descriptor .....	86
8.3	bus_info_block .....	88
8.4	Root directory entries .....	89
8.4.1	Bus_Dependent_Info .....	90
8.4.2	Module_Vendor_Id .....	90
8.4.3	Module_Hw_Version .....	90
8.4.4	Module_Spec_Id .....	91
8.4.5	Module_Sw_Version .....	91
8.4.6	Module_Dependent_Info .....	91
8.4.7	Node_Vendor_Id .....	91
8.4.8	Node_Hw_Version .....	91
8.4.9	Node_Spec_Id .....	91
8.4.10	Node_Sw_Version .....	92
8.4.11	Node_Capabilities .....	92
8.4.12	Node_Unique_Id .....	92
8.4.13	Node_Units_Extent .....	92
8.4.13.1	Node_Units_Extent immediate format .....	93
8.4.13.2	Node_Units_Extent offset format .....	94
8.4.14	Node_Memory_Extent .....	95
8.4.14.1	Node_Memory_Extent immediate format .....	95
8.4.14.2	Node_Memory_Extent offset format .....	96
8.4.15	Node_Dependent_Info .....	96

8.4.16	Unit_Directory .....	96
8.5	Unit directories .....	96
8.5.1	Unit_Spec_Id .....	97
8.5.2	Unit_Sw_Version .....	97
8.5.3	Unit_Dependent_Info .....	97
8.5.4	Unit_Location .....	97
8.5.5	Unit_Poll_Mask .....	98
8.6	Key definitions .....	98
8.7	company_ids .....	99
8.7.1	company_id assignments .....	99
8.7.2	company_id mappings .....	100
9.	Bus Standard requirements .....	101

## ANNEXES

A.	Bibliography (Informative) .....	103
B.	Bus topologies (Informative) .....	105
B.1	Specialized buses 1 .....	05
B.1.1	Multiple-bus topologies .....	105
B.1.2	Dual-port nodes .....	106
B.2	Fault retry protocols .....	106
B.2.1	Hardware fault recovery .....	106
B.2.2	Software fault recovery .....	107
C.	System initialization (Informative) .....	109
C.1	System initialization summary .....	109
C.2	Node address assignments .....	109
C.3	Processor-cache model .....	110
C.4	Address protection 1 .....	10
C.5	Power distribution models III	
D.	Bus transactions (Informative) .....	113
D.1	Transaction overview .....	113
D.2	Transaction components .....	113
D.3	Request subaction fields .....	113
D.4	Response subaction fields .....	114
E.	Bus bridges (Informative) 1 .....	17
E.1	Address-invariant mappings .....	117
E.2	Transaction forwarding .....	118
E.3	Transaction ordering .....	119
E.3.1	Split-response transaction ordering .....	119
E.3.2	Buffered-write transparency 1 .....	19
E.3.3	Weakly ordered move transactions .....	120
E.3.4	Queue-dependency deadlocks .....	121
E.4	Address domains .....	122
E.5	Protection boundaries .....	124
E.6	Coherence domains .....	124