

**Table of contents**

---

- European Foreword.....5**
- Introduction.....6**
- 1 Scope.....7**
- 2 Normative references .....8**
- 3 Terms, definitions and abbreviated terms.....9**
  - 3.1 Terms from other standards.....9
  - 3.2 Terms specific to the present standard .....9
  - 3.3 Abbreviated terms..... 18
  - 3.4 Nomenclature ..... 18
- 4 Principles .....20**
  - 4.1 General.....20
  - 4.2 Standard assumptions .....20
- 5 Requirements.....21**
  - 5.1 Reference power bus specifications .....21
  - 5.2 Functional/Source interface requirements.....23
    - 5.2.1 LCL/HLCL class .....23
    - 5.2.2 RLCL class .....23
    - 5.2.3 Current limitation section.....23
    - 5.2.4 Trip-off section .....24
    - 5.2.5 UVP section .....24
    - 5.2.6 Telecommand section features .....25
    - 5.2.7 Conditions at start-up/ switch-off .....25
    - 5.2.8 Telemetry section.....26
    - 5.2.9 Status section .....28
    - 5.2.10 Repetitive overload .....28
    - 5.2.11 Reverse current tolerance .....28
    - 5.2.12 Parallel connection.....29
    - 5.2.13 Switching options .....29
    - 5.2.14 LCL Switch dissipative failure.....31

5.2.15	Loss of LCL lines .....	32
5.2.16	Noise immunity .....	32
5.2.17	Output impedance envelope, when in limitation .....	32
5.2.18	Noise immunity feature .....	33
5.2.19	Output LCL load (Input load characteristic) .....	33
5.3	Functional/Load interface requirements .....	34
5.3.1	Nominal feature.....	34
5.3.2	Switch-on .....	34
5.3.3	LCL switch dissipative failure .....	35
5.3.4	Load test condition .....	35
5.3.5	User UVP at bus input side .....	35
5.4	Performance/Source interface requirements.....	36
5.4.1	Overall requirements.....	36
5.4.2	Start-up/Switch-off requirements .....	37
5.4.3	UVP .....	38
5.4.4	Switch-on capability .....	39
5.4.5	Voltage drop.....	40
5.4.6	Stability .....	40
5.4.7	Current Telemetry, accuracy.....	41
5.4.8	Current Telemetry, offset.....	41
5.4.9	Retrigger interval.....	42
5.4.10	di/dt limit on retrigger ON edge .....	42
5.4.11	di/dt limit on retrigger OFF edge.....	42
5.4.12	Status, accuracy .....	42
5.5	Performance/Load interface requirements .....	43
5.5.1	Load reverse current .....	43
5.5.2	Load characteristic.....	43
5.5.3	Source-load characteristic.....	44
5.5.4	Start-up surge input current.....	44
5.5.5	Internal load Input current limitation .....	45
<b>Annex A (informative) Requirements mapping .....</b>		<b>46</b>
<b>Bibliography.....</b>		<b>60</b>

**Figures**

Figure 3-1: LCL overload timing diagram (case 1) ..... 13  
Figure 3-2: LCL overload timing diagram (case 2) ..... 13  
Figure 3-3: Typical start-up current profile of a DC/DC converter attached to a LCL..... 14  
Figure 3-4: RLCL overload timing diagram ..... 14

**Tables**

Table 3-1: LCL classes ..... 15  
Table 3-2: RLCL classes ..... 16  
Table 3-3: HLCL classes ..... 17  
Table 5-1: Reference Power Bus Specifications ..... 22