

DIN EN 16602-60-12:2014-12 (E)

Space product assurance - Design, selection, procurement and use of die form monolithic microwave integrated circuits (MMICs); English version EN 16602-60-12:2014

Contents	Page
Foreword	6
Introduction	7
1 Scope	8
2 Normative references	9
3 Terms, definitions and abbreviated terms	10
3.1 Terms from other standards	10
3.2 Terms specific to the present document	10
3.3 Abbreviated terms	12
4 General requirements	14
4.1 Overview	14
4.2 Flight model MMIC dies lots procurement	14
4.3 Minimum quality requirements	14
5 Selection	15
5.1 General	15
5.1.1 Overview	15
5.1.2 Requirements	15
5.2 Process selection	16
5.3 Models, and design tools	16
6 Responsibilities	17
7 MMIC design	18
7.1 Principles of MMIC design	18
7.1.1 Overview	18
7.1.2 General	18
7.1.3 Number of design iterations	18
7.1.4 Design trade-offs	19
7.2 Design tasks	19
7.2.1 Electrical design specification	19
7.2.2 Design variations	19

7.2.3	Parasitic effects.....	19
7.2.4	Transient simulation.....	20
7.2.5	Thermal analysis.....	20
7.2.6	Sensitivity to temperature, process variation and supply voltages.....	20
7.2.7	Design testability.....	21
7.2.8	Design stability analysis.....	21
7.2.9	Maximum rating and robustness.....	21
7.2.10	Layout optimization.....	22
7.2.11	DRC or ERC.....	22
7.3	Design reviews.....	23
7.3.1	General.....	23
7.3.2	MMIC architecture.....	23
7.3.3	Schematic.....	23
7.3.4	Simulation results.....	23
7.3.5	Sensitivity and stability analysis.....	24
7.3.6	Derating.....	24
7.3.7	Layout.....	24
7.3.8	Tests matrix.....	24
7.3.9	Assembly.....	24
7.3.10	Compliance matrix.....	25
7.3.11	MMIC detail specification.....	25
7.3.12	Development plan.....	25
7.3.13	Design documentation.....	25
7.3.14	MMIC summary design sheet.....	25
8	Application approval.....	26
8.1	General.....	26
8.2	Test flow and test procedures.....	26
9	Procurement and LAT specification.....	28
10	Procurement.....	29
10.1	General.....	29
10.1.1	Overview.....	29
10.1.2	Methodology.....	29
10.2	Wafer screening and WAT.....	29
10.2.1	General.....	29
10.2.2	Wafer screening and WAT flows.....	29
10.2.3	Wafer manufacturing and control.....	30

10.2.4	Wafer acceptance test	31
10.2.5	Packaging	32
10.2.6	Deliverables	32
10.3	Dies incoming testing.....	33
10.3.1	General.....	33
10.3.2	Assembly test.....	33
10.3.3	Visual inspection	34
10.3.4	Electrical characterization	34
10.4	User LAT procurement sequences	35
10.4.1	General.....	35
10.4.2	Sequence A: process, design and application validated.....	38
10.4.3	Sequence B: process validated and new design or new application.....	38
10.4.4	Sequence C: process, design and application not validated.....	39
10.4.5	Sequence D: application approval testing	40
10.4.6	Destructive physical analysis after user LAT	40
10.5	Failure criteria and lot failure.....	41
Annex A (normative) MMIC electrical design specification - DRD		42
Annex B (normative) Compliance matrix for custom MMIC design - DRD		43
Annex C (normative) Design package document - DRD		44
Annex D (normative) MMIC summary design sheet - DRD		46
Annex E (normative) MMIC procurement specification - DRD.....		47
Annex F (normative) MMIC lot acceptance specification for user LAT - DRD		48
Annex G (normative) MMIC visual inspection summary sheet - DRD		50
Annex H (informative) References		51
Bibliography.....		52
 Figures		
Figure 10-1:	Wafer screening and WAT	30
Figure 10-2:	Dies or die incoming testing	34
Figure 10-3:	Acceptance flow for flight model die lots.....	35
Figure 10-4:	User LAT flow.....	37
 Tables		
Table 6-1:	Customer and supplier responsibilities for the “foundry” and “catalogue” modes.....	17
Table 8-1:	CTA tests and procedures for testing in sequence D.....	27