

ISO/IEC TR 14496-9:2009-02 (E)

Information technology - Coding of audio-visual objects - Part 9: Reference hardware description

Contents		Page
Foreword		v
Introduction		vii
1	Scope	1
2	Copyright disclaimer for HDL software modules	1
3	Abbreviated terms	2
4	HDL software availability	2
5	HDL coding format and standards	2
5.1	HDL standards and libraries	2
5.2	Conditions and tools for the synthesis of HDL modules	3
5.3	Conformance with the reference software	3
6	Integrated Framework supporting the "Virtual Socket" between HDL modules described in Part 9 and the MPEG Reference Software (Implementation 1)	3
6.1	Introduction	3
6.2	Addressing	4
6.3	Memory Map	4
6.4	Hardware Accelerator Interface	6
6.5	User Hardware Accelerator Sockets	12
7	Integrated Framework supporting the "Virtual Socket" between HDL modules described in Part 9 and the MPEG Reference Software (Implementation 2)	14
7.1	Introduction	14
7.2	Development Example of a Typical Module : Calc_Sum_Product Module	14
7.3	Second Example of a Typical Module : fifo_transfer module	18
7.4	Integrating the Multi-Modules within the Framework	23
7.5	Calc_Sum_Product Module Controller (memory data transfer)	30
7.6	Simulation of the whole system	44
7.7	Debug Menu	46
8	Integrated Framework supporting the "Virtual Socket" between HDL modules described in Part 9 and the MPEG Reference Software (Implementation 3)	47
8.1	An Integrated Virtual Socket Hardware-Accelerated Co-design Platform for MPEG-4	47
8.2	Reference for Virtual Socket API Function Calls	72
8.3	Tutorial on the Integrated Virtual Socket Hardware-Accelerated Co-design Platform for MPEG-4 Part 9 Implementation 3	95
8.4	An Integration of the MPEG-4 Part 10/AVC DCT/Q Hardware Module into the Virtual Socket Co-design Platform	140
8.5	Migrating Virtual Socket Hardware-Accelerated Co-design Platform From WildCard-II to WildCard-4	153
9	Integrated Framework supporting the "Virtual Socket" between HDL modules described in Part 9 and the MPEG Reference Software: Implementation 4 - Virtual Memory Extension	167
9.1	Introduction	167
9.2	Overview of the "Virtual Socket Platform" implementation 4	167

9.3	Development information	171
9.4	Technical details	172
9.5	How to build the platform	196
9.6	Simulation of the platform	203
9.7	Synthesis of the platform	209
9.8	Building the platform system software	212
9.9	How to use the platform	214
9.10	Understanding VHDL code	216
9.11	Appendix	220
9.12	Glossary	222
10	HDL MODULES	225
10.1	INVERSE QUANTIZER HARDWARE IP BLOCK FOR MPEG-4 PART 2	225
10.2	2-D IDCT HARDWARE IP BLOCK FOR MPEG-4 PART 2	232
10.3	VLD+IQ+IDCT for MPEG-4 Part 2	242
10.4	A SYSTEM C MODEL FOR 2X2 HADAMARD TRANSFORM AND QUANTIZATION FOR MPEG-4 PART 10	247
10.5	A VHDL HARDWARE BLOCK FOR 2X2 HADAMARD TRANSFORM AND QUANTIZATION WITH APPLICATION TO MPEG-4 PART 10 AVC	256
10.6	A SYSTEMC MODEL FOR 4X4 HADAMARD TRANSFORM AND QUANTIZATION FOR MPEG-4 PART 10	262
10.7	A VHDL HARDWARE IP BLOCK FOR 4X4 HADAMARD TRANSFORM AND QUANTIZATION FOR MPEG-4 PART 10 AVC	269
10.8	A HARDWARE BLOCK FOR THE MPEG-4 PART 10 4X4 DCT-LIKE TRANSFORMATION AND QUANTIZATION	275
10.9	A SYSTEMC MODEL FOR THE MPEG-4 PART 10 4X4 DCT-LIKE TRANSFORMATION AND QUANTIZATION	281
10.10	A 8X8 INTEGER APPROXIMATION DCT TRANSFORMATION AND QUANTIZATION SYSTEMC IP BLOCK FOR MPEG-4 PART 10 AVC	289
10.11	INTEGER APPROXIMATION OF 8X8 DCT TRANSFORMATION AND QUANTIZATION, A HARDWARE IP BLOCK FOR MPEG-4 PART 10 AVC	299
10.12	A VHDL CONTEXT-BASED ADAPTIVE VARIABLE LENGTH CODING (CAVLC) IP BLOCK FOR MPEG-4 PART 10 AVC	306
10.13	A VERILOG HARDWARE IP BLOCK FOR SA-DCT FOR MPEG-4	311
10.14	A VERILOG HARDWARE IP BLOCK FOR SA-IDCT FOR MPEG-4	322
10.15	A VERILOG HARDWARE IP BLOCK FOR 2D-DCT (8X8)	335
10.16	SHAPE CODING BINARY MOTION ESTIMATION HARDWARE ACCELERATION MODULE	344
10.17	A SIMD ARCHITECTURE FOR FULL SEARCH BLOCK MATCHING ALGORITHM	358
10.18	HARDWARE MODULE FOR MOTION ESTIMATION (4xPE)	367
10.19	A IP BLOCK FOR H.264/AVC QUARTER PEL FULL SEARCH VARIABLE BLOCK MOTION ESTIMATION	381
10.20	AN IP BLOCK FOR VARIABLE BLOCK SIZE MOTION ESTIMATION IN H.264/MPEG-4 AVC	389
10.21	An IP Block for MPEG-4 Part 10 AVC Deblocking Filter	400
10.22	A HW BLOCK FOR MPEG-4 PART 10 AVC CONTEXT ADAPTIVE VARIABLE LENGTH CODING (CAVLC)	407
10.23	HARDWARE IMPLEMENTATION OF FULL SEARCH MPEG-4 PART 10 AVC MOTION ESTIMATION	421
Annex A (Informative)	Specification of directory structure for reference SW, HDL and documentation files of MPEG-4 Part 9 Reference HW Description	433
A.1	Introduction	433
A.2	Directory Structure of TR SW Modules	433
CVS Module Name		434
Integration Framework Version		435
Reference Software Version and Modifications		435
Annex B (Informative)	Tutorial on Part 9 CVS Client Installation & Operation	436

Annex C (Informative) Additional utility software446
Annex D (Informative) Providers of reference hardware code447
Bibliography448