

ISO 21111-6:2021-11 (E)

Road vehicles - In-vehicle Ethernet - Part 6: Electrical 100-Mbit/s physical entity requirements and conformance test plan

Contents		Page
	Foreword.....	vi
	Introduction.....	vii
1	Scope	1
2	Normative references	1
3	Terms and definitions	1
4	Symbols and abbreviated terms	2
	4.1 Symbols.....	2
	4.2 Abbreviated terms.....	2
5	Conventions	4
6	Wake-up and sleep features	4
	6.1 Extension of physical coding sub-layer.....	4
	6.2 Service primitives and interfaces.....	6
	6.3 Power sequencing states.....	7
	6.4 Command definitions.....	8
	6.4.1 General.....	8
	6.4.2 Low power sleep (LPS).....	8
	6.4.3 Wake-up request (WUR).....	9
	6.4.4 Wake-up pulse (WUP).....	9
	6.5 Generation of scrambling bits $s_{dn}[2:0]$	9
	6.6 PCS PHY control state diagram.....	10
7	CTP test system and CTC structure	12
	7.1 General.....	12
	7.2 Test system set-up – Transmit test system.....	13
	7.3 Test system set-up – Receive test system.....	14
	7.4 CTC structure.....	15
8	PHY – Control IUT conformance test plan (with MII access)	16
	8.1 PHY – Group 1: PHY control and timers (with MII access).....	16
	8.1.1 Overview.....	16
	8.1.2 CTC_4.1.1 – PMA reset (with MII access).....	16
	8.1.3 CTC_4.1.2 – Value of <code>minwait_timer</code> – <code>minwait_timer</code> in TRAINING state (with MII access).....	17
	8.1.4 CTC_4.1.3 – Value of <code>maxwait_timer</code> (with MII access).....	21
	8.1.5 CTC_4.1.4 – Value of <code>stabilize_timer</code> (with MII access).....	22
	8.2 PHY – Group 2: PHY control state diagram (with MII access).....	23
	8.2.1 Overview.....	23
	8.2.2 CTC_4.2.1 – PHY control state diagram - DISABLE TRANSMITTER state (with MII access).....	23
	8.2.3 CTC_4.2.2 – PHY control state diagram - SLAVE SILENT state (with MII access).....	24
	8.2.4 CTC_4.2.3 – PHY control state diagram – TRAINING state (with MII access).....	25
	8.2.5 CTC_4.2.4 – PHY control state diagram – SEND IDLE state (with MII access).....	28
	8.2.6 CTC_4.2.5 – PHY control state diagram – SEND IDLE OR DATA state (with MII access).....	31
	8.3 PHY – Group 3: PHY link monitor state diagram (with MII access).....	35
	8.3.1 Overview.....	35
	8.3.2 CTC_4.3.1 – Link monitor state diagram – IUT does not enter the LINK OK state (with MII access).....	36

9	PCS – IUT conformance test plan (with MII access)	38
9.1	PCS – Group 1: PCS transmit (with MII access).....	38
9.1.1	Overview.....	38
9.1.2	CTC_3.1.1 – PCS signalling (with MII access).....	39
9.1.3	CTC_3.1.2 – PCS reset (with MII access).....	41
9.1.4	CTC_3.1.3 – PCS transmit proper SSD (with MII access).....	41
9.1.5	CTC_3.1.4 – PCS transmit proper ESD (with MII access).....	42
9.1.6	CTC_3.1.5 – PCS transmit ESD with tx_error (with MII access).....	43
9.1.7	CTC_3.1.6 – PCS transmission of stuff bits (with MII access).....	44
9.1.8	CTC_3.1.7 – PCS tx_error (with MII access).....	44
9.2	PCS – Group 2: PCS transmit state diagram (with MII access).....	46
9.2.1	Overview.....	46
9.2.2	CTC_3.2.1 – PCS transmit state diagram - SEND IDLE state (with MII access).....	46
9.2.3	CTC_3.2.2 – PCS transmit state diagram - SSD1 VECTOR and SSD2 VECTOR states (with MII access).....	47
9.2.4	CTC_3.2.3 – PCS transmit state diagram - SSD3 VECTOR state (with MII access).....	47
9.2.5	CTC_3.2.4 – PCS transmit state diagram - TRANSMIT DATA state (with MII access).....	49
9.2.6	CTC_3.2.5 – PCS transmit state diagram - ESD1 VECTOR state (with MII access).....	50
9.2.7	CTC_3.2.6 – PCS transmit state diagram - ESD2 VECTOR state (with MII access).....	50
9.2.8	CTC_3.2.7 – PCS transmit state diagram - ESD3 VECTOR state (with MII access).....	51
9.2.9	CTC_3.2.8 – PCS transmit state diagram - ERR ESD1 VECTOR state (with MII access).....	52
9.2.10	CTC_3.2.9 – PCS transmit state diagram - ERR ESD2 VECTOR state (with MII access).....	53
9.2.11	CTC_3.2.10 – PCS transmit state diagram - ERR ESD3 VECTOR state (with MII access).....	54
9.3	PCS – Group 3: PCS receive (with MII access).....	54
9.3.1	Overview.....	54
9.3.2	CTC_3.3.1 – PCS receive signalling (with MII access).....	54
9.3.3	CTC_3.3.2 – PCS automatic polarity detection (with MII access).....	55
9.3.4	CTC_3.3.3 – PCS receive SSD (with MII access).....	56
9.3.5	CTC_3.3.4 – PCS receive ESD (with MII access).....	57
9.3.6	CTC_3.3.5 – PCS receive ERR ESD3 (with MII access).....	57
9.3.7	CTC_3.3.6 – PCS reception of stuff bits (with MII access).....	58
9.3.8	CTC_3.3.7 – PCS de-interleave ternary pairs (with MII access).....	59
9.4	PCS – Group 4: PCS receive state diagram (with MII access).....	59
9.4.1	Overview.....	59
9.4.2	CTC_3.4.1 – PCS receive state diagram (with MII access) - IDLE state.....	59
9.4.3	CTC_3.4.2 – PCS receive state diagram (with MII access) - CHECK SSD2 state.....	60
9.4.4	CTC_3.4.3 – PCS receive state diagram (with MII access) - CHECK SSD3 state.....	61
9.4.5	CTC_3.4.4 – PCS receive state diagram (with MII access) - SSD state.....	61
9.4.6	CTC_3.4.5 – PCS receive state diagram (with MII access) - BAD SSD state.....	62
9.4.7	CTC_3.4.6 – PCS receive state diagram (with MII access) - FIRST SSD state.....	63
9.4.8	CTC_3.4.7 – PCS receive state diagram (with MII access) - SECOND SSD state.....	64
9.4.9	CTC_3.4.8 – PCS receive state diagram (with MII access) - THIRD SSD state.....	65
9.4.10	CTC_3.4.9 – PCS receive state diagram (with MII access) - DATA state.....	65
9.4.11	CTC_3.4.10 – PCS receive state diagram (with MII access) - CHECK ESD2 state.....	66
9.4.12	CTC_3.4.11 – PCS receive state diagram (with MII access) - CHECK ESD3 state.....	67
9.4.13	CTC_3.4.12 – PCS receive state diagram (with MII access) - BAD ESD2 state.....	68
9.4.14	CTC_3.4.13 – PCS receive state diagram (with MII access) - BAD END and RX ERROR states.....	69
9.5	PCS – Group 5: PCS JAB state diagram (with MII access).....	70
9.5.1	Overview.....	70
9.5.2	CTC_3.5.1 – PCS JAB state diagram (with MII access) - rcv_max_timer	70
10	PMA – IUT requirements and conformance test plan (with MII access)	71

10.1	PMA – Group 1: PMA electrical measurements (with MII access).....	71
10.1.1	Overview.....	71
10.1.2	CTC_5.1.1 – PMA maximum transmitter output droop (with MII access).....	71
10.1.3	CTC_5.1.2 – PMA transmitter distortion (with MII access).....	72
10.1.4	CTC_5.1.3 – PMA transmitter timing jitter (with MII access).....	73
10.1.5	CTC_5.1.4 – PMA transmitter power spectral density (PSD) (with MII access).....	74
10.1.6	CTC_5.1.5 – PMA transmit clock frequency (with MII access).....	76
10.1.7	CTC_5.1.6 – PMA MDI return loss (with MII access).....	77
10.1.8	CTC_5.1.7 – PMA MDI mode conversion loss (with MII access).....	79
10.1.9	CTC_5.1.8 – PMA transmitter peak differential output (with MII access).....	82
10.2	PMA – Group 2: PMA receive tests (with MII access).....	83
10.2.1	Group 2 overview.....	83
10.2.2	CTC_5.2.1 – PMA bit error rate verification (with MII access).....	83
10.2.3	CTC_5.2.2 – PMA receiver frequency tolerance (with MII access).....	84
10.2.4	CTC_5.2.3 – PMA alien crosstalk noise rejection (with MII access).....	85
	Annex A (informative) PHY control – Test suite.....	87
	Annex B (normative) PCS – Test suite.....	91
	Annex C (normative) PMA – Test system set-ups.....	110
	Bibliography.....	123