

# ISO 21806-13:2021-05 (E)

## Road vehicles - Media Oriented Systems Transport (MOST) - Part 13: 50-Mbit/s balanced media physical layer conformance test plan

---

<b>Contents</b>		<b>Page</b>
Foreword		v
Introduction		vi
<b>1</b>	<b>Scope</b>	<b>1</b>
<b>2</b>	<b>Normative references</b>	<b>1</b>
<b>3</b>	<b>Terms and definitions</b>	<b>1</b>
<b>4</b>	<b>Symbols and abbreviated terms</b>	<b>2</b>
4.1	Symbols	2
4.2	Abbreviated terms	2
<b>5</b>	<b>Conventions</b>	<b>3</b>
<b>6</b>	<b>Operating conditions and measurement tools, requested accuracy</b>	<b>3</b>
6.1	Operating conditions	3
6.2	Apparatus — Measurement tools, requested accuracy	3
<b>7</b>	<b>Electrical characteristics</b>	<b>4</b>
<b>8</b>	<b>Balanced media characteristics</b>	<b>4</b>
8.1	Threshold for detection of alignment and transferred jitter	4
8.2	RMS signal amplitude	4
8.3	PSD of SP2 output signal	5
8.4	Attenuation of electrical interconnect	7
8.4.1	General	7
8.4.2	Test procedure general	8
8.4.3	Example set-up test procedure	8
8.4.4	Test procedure for data acquisition	8
8.4.5	Impact of attenuation on the data signal	9
8.5	Characteristic impedance of balanced media	10
8.6	RL of PCB interfaces	13
8.7	Receive tolerance	15
8.7.1	General	15
8.7.2	Pattern generator	15
8.7.3	Arbitrary signal generator	16
8.7.4	Cable assembly or its analogue representation	16
8.7.5	Stimulus creation for SP3	16
<b>9</b>	<b>Measurement of phase variation</b>	<b>18</b>
9.1	General	18
9.2	Measuring alignment jitter	20
9.3	Measuring transferred jitter	23
<b>10</b>	<b>Test set-ups</b>	<b>26</b>
10.1	General	26
10.2	Set-ups for SP2 link quality	26
10.3	Set-ups for SP3 link quality	28
10.4	Set-ups for SP3 receive tolerance	30
<b>11</b>	<b>Power-on and power-off</b>	<b>31</b>
11.1	General	31
11.2	Measuring EBC parameters	32
11.2.1	Measuring EBC parameters – Test set-up	32
11.2.2	Measuring EBC parameters – Signal charts	33
11.2.3	Measuring EBC parameters – Test sequences	33

11.3	Measuring BEC parameters .....	35
11.3.1	Measuring BEC parameters – Test set-up .....	35
11.3.2	Measuring BEC parameters – Signal chart .....	37
11.3.3	Measuring BEC parameters – Test sequences .....	37
<b>12</b>	<b>Detecting bit rate (frequency reference) .....</b>	<b>40</b>
<b>13</b>	<b>System performance .....</b>	<b>41</b>
13.1	General .....	41
13.2	SP3 receiver tolerance .....	41
13.3	TimingMaster delay tolerance .....	41
<b>14</b>	<b>Conformance test of 50-Mbit/s balanced media physical layer .....</b>	<b>44</b>
14.1	Location of interfaces .....	44
14.2	Control signals .....	44
14.3	Limited access to specification points .....	45
14.4	Parameter overview .....	45
<b>15</b>	<b>Limited physical layer conformance .....</b>	<b>45</b>
15.1	Overview .....	45
15.2	Test set-up .....	46
15.3	Generating test signals for the IUT input section SP3 .....	47
15.4	Analysis of test results .....	47
15.5	Test flow overview .....	47
15.6	Measurement of SP3 input signal of the IUT .....	48
15.7	Measurement of SP2 output signal of the IUT .....	49
15.8	Measurement of RL .....	49
15.9	Functional test of wake-up and shutdown .....	49
<b>16</b>	<b>Direct physical measuring accuracy .....</b>	<b>50</b>
<b>Annex A (informative) Limited physical layer conformance for development tools .....</b>		<b>51</b>
<b>Annex B (normative) SP3 stress conditions .....</b>		<b>52</b>
<b>Annex C (informative) Test fixture .....</b>		<b>53</b>
<b>Annex D (informative) Overview on test modes .....</b>		<b>56</b>
<b>Bibliography .....</b>		<b>57</b>