Table of Contents

Foreword 27
Introduction 28
Summary 33
Introduction 33

I Partition I - Input/Output Logical Specification 38
I.1 Overview 38
I.2 Contents 38
I.3 Normative References 38

1 Chapter 1 - System Models 38
1.1 Processing Element Models 38
1.1.1 Processor-Memory Processing Element Model 39
1.1.2 Integrated Processor-Memory Processing Element Model 39
1.1.3 Memory-Only Processing Element Model 40
1.1.4 Processor-Only Processing Element 40
1.1.5 I/O Processing Element 40
1.1.6 Switch Processing Element 41
1.2 System Issues 41
1.2.1 Operation Ordering 41
1.2.2 Transaction Delivery 42
1.2.3 Deadlock Considerations 43

2 Chapter 2 - Operation Descriptions 43
2.1 I/O Operations Cross Reference 44
2.2 I/O Operations 44
2.2.1 Read Operations 45
2.2.2 Write and Streaming-Write Operations 45
2.2.3 Write-With-Response Operations 45
2.2.4 Atomic (Read-Modify-Write) Operations 46
2.3 System Operations 46
2.3.1 Maintenance Operations 46
2.4 Endian, Byte Ordering, and Alignment 46

3 Chapter 3 - Packet Format Descriptions 48
3.1 Request Packet Formats 48
3.1.1 Addressing and Alignment 48
3.1.2 Field Definitions for All Request Packet Formats 48
3.1.3 Type 0 Packet Format (Implementation-Defined) 51
3.1.4 Type 1 Packet Format (Reserved) 51
3.1.5 Type 2 Packet Format (Request Class) 51
3.1.6 Type 3–4 Packet Formats (Reserved) 52
3.1.7 Type 5 Packet Format (Write Class) 52
3.1.8 Type 6 Packet Format (Streaming-Write Class) 53
3.1.9 Type 7 Packet Format (Reserved) 53
3.1.10 Type 8 Packet Format (Maintenance Class) 53
3.1.11 Type 9–11 Packet Formats (Reserved) 55

3.2 Response Packet Formats 55
3.2.1 Field Definitions for All Response Packet Formats 56
3.2.2 Type 12 Packet Format (Reserved) 56
3.2.3 Type 13 Packet Format (Response Class) 56
3.2.4 Type 14 Packet Format (Reserved) 56

4 Chapter 4 - Input/Output Registers 57
4.1 Register Summary. 57
4.2 Reserved Register and Bit Behavior 57
4.3 Extended Features Data Structure. 58
4.4 Capability Registers (CARs) 59
4.4.1 Device Identity CAR (Offset 0x0 Word 0). 59
4.4.2 Device Information CAR (Offset 0x0 Word 1) 59
4.4.3 Assembly Identity CAR (Offset 0x8 Word 0). 59
4.4.4 Assembly Information CAR (Offset 0x8 Word 1) 60
4.4.5 Processing Element Features CAR (Offset 0x10 Word 0) 60
4.4.6 Switch Port Information CAR (Offset 0x10 Word 1) 61
4.4.7 Source Operations CAR (Offset 0x18 Word 0). 61
4.4.8 Destination Operations CAR (Offset 0x18 Word 1) 61
4.5 Command and Status Registers (CSRs) 62
4.5.1 Write Port CSR (Offset 0x40 Word 1) 62
4.5.2 Processing Element Logical Layer Control CSR (Offset 0x48 Word 1). 63
4.5.3 Local Configuration Space Base Address 0 CSR (Offset 0x58 Word 0). 63
4.5.4 Local Configuration Space Base Address 1 CSR (Offset 0x58 Word 1) 64

II Partition II - Message Passing Logical Specification 66
II.1 Overview. 66
II.2 Contents 66

1 Chapter 1 - System Models 66
1.1 Processing Element Models 66
1.1.1 Processor-Memory Processing Element Model. 67
1.1.2 Integrated Processor-Memory Processing Element Model 67
1.1.3 Memory-Only Processing Element Model 68
1.1.4 Processor-Only Processing Element 68
1.1.5 I/O Processing Element 68
1.1.6 Switch Processing Element 69
1.2 Message Passing System Model 69
1.2.1 Data Message Operations 69
1.2.2 Doorbell Message Operations 70
1.3 System Issues 70
1.3.1 Operation Ordering 70
1.3.2 Transaction Delivery 70
1.3.3 Deadlock Considerations 71

Table of Contents

2 Chapter 2 - Operation Descriptions 71
2.1 Message Passing Operations Cross Reference 72
2.2 Message Passing Operations 72
2.2.1 Doorbell Operations 72
2.2.2 Data Message Operations 72
2.3 Endian, Byte Ordering, and Alignment 73

3 Chapter 3 - Packet Format Descriptions 74
3.1 Request Packet Formats 74
3.1.1 Field Definitions for All Request Packet Formats 74
3.1.2 Type 0 Packet Format (Implementation-Defined) 75
3.1.3 Type 1–9 Packet Formats (Reserved) 75
3.1.4 Type 10 Packet Formats (Doorbell Class) 75
3.1.5 Type 11 Packet Format (Message Class) 75
3.2 Response Packet Formats 76
3.2.1 Field Definitions for All Response Packet Formats 77
3.2.2 Type 12 Packet Format (Reserved) 77
3.2.3 Type 13 Packet Format (Response Class) 77
3.2.4 Type 14 Packet Format (Reserved) 78
3.2.5 Type 15 Packet Format (Implementation-Defined) 78

4 Chapter 4 - Message Passing Registers 78
4.1 Register Summary 78
4.2 Reserved Register and Bit Behavior 79
4.3 Capability Registers (CARs) 80
4.3.1 Processing Element Features CAR (Offset 0x10 Word 0) 80
4.3.2 Source Operations CAR (Offset 0x18 Word 0) 80
4.3.3 Destination Operations CAR (Offset 0x18 Word 1) 81
4.4 Command and Status Registers (CSRs) 81
4.4.1 Mailbox CSR (Offset 0x40 Word 0) 81
4.4.2 Doorbell CSR (Offset 0x40 Word 1) 83
Annex A (informative) Interface Management 84
A.1 Link Initialization and Maintenance Mechanism 84
A.1.1 Input port training state machine 84
A.1.2 Output port training state machine 86
A.2 Packet Retry Mechanism 89
A.2.1 Input port retry recovery state machine 89
A.2.2 Output port retry recovery state machine 90
A.3 Error Recovery 92
A.3.1 Input port error recovery state machine 92
A.3.2 Output port error recovery state machine 94

III Partition III - Common Transport Specification 98
III.1 Overview 98
III.2 Contents 98

Table of Contentss

1 Chapter 1 - Transport Format Description 98
1.1 System Topology 98
1.1.1 Switch-Based Systems 98
1.1.2 Ring-Based Systems 99
1.2 System Packet Routing 99
1.3 Field Alignment and Definition 100
1.3.1 Routing Maintenance Packets 100

2 Chapter 2 - Common Transport Registers 101
2.1 Register Summary 101
2.2 Reserved Register and Bit Behavior 102
2.3 Capability Registers (CARs) 103
2.3.1 Processing Element Features CAR (Offset 0x10 Word 0) 103
2.4 Command and Status Registers (CSRs) 103
2.4.1 Base Device ID CSR (Offset 0x60 Word 0) 103
2.4.2 Host Base Device ID Lock CSR (Offset 0x68 Word 0) 103
2.4.3 Component Tag CSR (Offset 0x68 Word 1) 104

IV Partition IV - Physical Layer 8/16 LP-LVDS Specification 106
IV.1 Overview 106
IV.2 Contents 106

1 Chapter 1 - Physical Layer Protocol 106
1.1 Packet Exchange Protocol 106
1.1.1 Packet and Control Alignment 107
1.1.2 Acknowledge Identification 107
1.2 Field Placement and Definition 108
1.2.1 Flow Control Fields Format 108
1.2.2 Packet Priority and Transaction Request Flows 109
1.2.3 Transaction and Packet Delivery 110
1.2.4 Resource Allocation 112
1.2.5 Flow Control Mode Negotiation 117
1.3 Error Detection and Recovery 117
1.3.1 Control Symbol Protection 117
1.3.2 Packet Protection 117
1.3.3 Lost Packet Detection 118
1.3.4 Implementation Note: Transactional Boundaries 118
1.3.5 Link Behavior Under Error 119
1.3.6 CRC Operation 120
1.3.7 CRC Code 122
1.3.8 Maximum Packet Size 123
1.4 Link Maintenance Protocol 123
1.4.1 Command Descriptions 123
1.4.2 Status Descriptions 124

Table of Contents

2 Chapter 2 - Packet and Control Symbol Transmission 125
2.1 Packet Start and Control Symbol Delineation 125
2.2 Packet Termination 127
2.3 Packet Pacing 128
2.4 Embedded Control Symbols 129
2.5 Packet to Port Alignment 129
2.6 System Maintenance 133
2.6.1 Port and Link Initialization 133
2.6.2 Multicast-Event 136
2.7 Power Management 136

3 Chapter 3 - Control Symbol Formats 137
3.1 Acknowledgment Control Symbol Formats 137
3.1.1 Packet-Accepted Control Symbol 137
3.1.2 Packet-Retry Control Symbol 137
3.1.3 Packet-Not-Accepted Control Symbol 138
3.1.4 Canceling Packets 139
3.2 Packet Control Symbol Formats 139
3.3 Link Maintenance Control Symbol Formats 140
3.4 Reserved Symbol Formats 142
3.5 Control Symbol to Port Alignment 142

4 Chapter 4 - 8/16 LP-LVDS Registers 143
4.1 Generic End Point Devices 143
4.1.1 Register Map 144
4.1.2 Command and Status Registers (CSRs) 145
4.2 Generic End Point Devices, software assisted error recovery option 149
4.2.1 Register Map 149
4.2.2 Command and Status Registers (CSRs) 150
4.3 Generic End Point Free Devices 155
4.3.1 Register Map 155
4.3.2 Command and Status Registers (CSRs) 155

5 Chapter 5 - System Clocking Considerations 160
5.1 Example Clock Distribution 160
5.2 Elasticity Mechanism 161

6 Chapter 6 - Board Routing Guidelines 161
6.1 Impedance 161
6.2 Skew 162
6.3 PCB Stackup 162
6.4 Termination 163
6.5 Additional Considerations 163
6.5.1 Single Board Environments 163
6.5.2 Single Connector Environments 163
6.5.3 Backplane Environments 163
6.6 Recommended pin escape ordering 163

7 Chapter 7 - Signal Descriptions 166
7.1 Signal Definitions 166
7.2 RapidIO Interface Diagrams 168

8 Chapter 8 - Electrical Specifications 170
8.1 Overview 170
8.2 DC Specifications 170
8.3 AC Specifications 171
8.3.1 Concepts and Definitions 172
8.3.2 Driver Specifications 173
8.3.3 Receiver Specifications 178
Annex A (informative) Message Passing Interface 185
A.1 Definitions and Goals 185
A.2 Message Operations 185
A.3 Inbound Mailbox Structure 186
A.3.1 Simple Inbox 186
A.3.2 Extended Inbox 187
A.3.3 Received Messages 188
A.4 Outbound Message Queue Structure 189
A.4.1 Simple Outbox 189
A.4.2 Extended Outbox 189

V Partition V - Globally Shared Memory Logical Specification 192

1 Chapter 1 - Globally Shared Memory 192
1.1 Overview 192
1.1.1 Memory System 192
1.2 Features of the Globally Shared Memory Specification 193
1.2.1 Functional Features 194
1.2.2 Physical Features 194
1.2.3 Performance Features 194
1.3 Contents 194
1.4 Terminology 195
1.5 Conventions 195

2 Chapter 2 - System Models 195
2.1 Processing Element Models 195
2.1.1 Processor-Memory Processing Element Model 196
2.1.2 Integrated Processor-Memory Processing Element Model 196
2.1.3 Memory-Only Processing Element Model 197
2.1.4 Processor-Only Processing Element 197
2.1.5 I/O Processing Element 197
2.1.6 Switch Processing Element 198
2.2 Programming Models 198
2.2.1 Globally Shared Memory System Model 198
2.2.2 Software-Managed Cache Coherence Programming Model 199

2.3 System Issues 199
2.3.1 Operation Ordering 199
2.3.2 Transaction Delivery 200
2.3.3 Deadlock Considerations 200

3 Chapter 3 - Operation Descriptions 200
3.1 GSM Operations Cross Reference 201
3.2 GSM Operations 202
3.2.1 Read Operations 202
3.2.2 Instruction Read Operations 203
3.2.3 Read-for-Ownership Operations 205
3.2.4 Data Cache Invalidate Operations 206
3.2.5 Castout Operations 207
3.2.6 TLB Invalidate-Entry Operations 207
3.2.7 TLB Invalidate-Entry Synchronization Operations 207
3.2.8 Instruction Cache Invalidate Operations 208
3.2.9 Data Cache Flush Operations 208
3.2.10 I/O Read Operations 210
3.3 Endian, Byte Ordering, and Alignment 211

4 Chapter 4 - Packet Format Descriptions 212
4.1 Request Packet Formats 212
4.1.1 Addressing and Alignment 213
4.1.2 Data Payloads 213
4.1.3 Field Definitions for All Request Packet Formats 214
4.1.4 Type 0 Packet Format (Implementation-Defined) 217
4.1.5 Type 1 Packet Format (Intervention-Request Class) 217
4.1.6 Type 2 Packet Format (Request Class) 217
4.1.7 Type 3–4 Packet Formats (Reserved) 218
4.1.8 Type 5 Packet Format (Write Class) 218
4.1.9 Type 6–11 Packet Formats (Reserved) 219
4.2 Response Packet Formats 219
4.2.1 Field Definitions for All Response Packet Formats 219
4.2.2 Type 12 Packet Format (Reserved) 220
4.2.3 Type 13 Packet Format (Response Class) 220
4.2.4 Type 14 Packet Format (Reserved) 221
4.2.5 Type 15 Packet Format (Implementation-Defined) 221

5 Chapter 5 - Globally Shared Memory Registers 221
5.1 Register Summary 221
5.2 Reserved Register and Bit Behavior 221
5.3 Capability Registers (CARs) 222
5.3.1 Source Operations CAR (Offset 0x18 Word 0) 223
5.3.2 Destination Operations CAR (Offset 0x18 Word 1) 223

6 Chapter 6 - Communication Protocols 224
6.1 Definitions 224
6.1.1 General Definitions 224
6.1.2 Request and Response Definitions 225
6.2 Operation to Protocol Cross Reference 226
6.3 Read Operations 227
6.3.1 Internal Request State Machine 227
6.3.2 Response State Machine 227
6.3.3 External Request State Machine 229
6.4 Instruction Read Operations 230
6.4.1 Internal Request State Machine 230
6.4.2 Response State Machine 231
6.4.3 External Request State Machine 232
6.5 Read for Ownership Operations 232
6.5.1 Internal Request State Machine 233
6.5.2 Response State Machine 233
6.5.3 External Request State Machine 236
6.6 Data Cache and Instruction Cache Invalidate Operations 237
6.6.1 Internal Request State Machine 237
6.6.2 Response State Machine 238
6.6.3 External Request State Machine 239
6.7 Castout Operations 239
6.7.1 Internal Request State Machine 239
6.7.2 Response State Machine 240
6.7.3 External Request State Machine 240
6.8 TLB Invalidate Entry, TLB Invalidate Entry Synchronize Operations 240
6.8.1 Internal Request State Machine 240
6.8.2 Response State Machine 240
6.8.3 External Request State Machine 241
6.9 Data Cache Flush Operations 241
6.9.1 Internal Request State Machine 241
6.9.2 Response State Machine 241
6.9.3 External Request State Machine 244
6.10 I/O Read Operations 244
6.10.1 Internal Request State Machine 245
6.10.2 Response State Machine 245
6.10.3 External Request State Machine 246

7 Chapter 7 - Address Collision Resolution Tables 248
7.1 Resolving an Outstanding READ_HOME Transaction 248
7.2 Resolving an Outstanding IREAD_HOME Transaction 249
7.3 Resolving an Outstanding READ_OWNER Transaction 249
7.4 Resolving an Outstanding READ_TO_OWN_HOME Transaction 250
7.5 Resolving an Outstanding READ_TO_OWN_OWNER Transaction 252
7.6 Resolving an Outstanding DKILL_HOME Transaction 253
7.7 Resolving an Outstanding DKILL_SHARER Transaction 254
7.8 Resolving an Outstanding IKILL_HOME Transaction 255

7.9 Resolving an Outstanding IKILL_SHARER Transaction . . . 256
7.10 Resolving an Outstanding CASTOUT Transaction . . . 257
7.11 Resolving an Outstanding TLBIE or TLBSYNC Transaction . . . 258
7.12 Resolving an Outstanding FLUSH Transaction . . . 258
7.13 Resolving an Outstanding IO_READ_HOME Transaction . . . 260
7.14 Resolving an Outstanding IO_READ_OWNER Transaction . . . 262
Glossary of Terms and Abbreviations . . . 265

VI Partition VI - Physical Layer 1x/4x LP-Serial Specification . . . 270

1 Chapter 1 - Overview . . . 270
1.1 Packets . . . 270
1.2 Control Symbols . . . 270
1.3 PCS and PMA Layers . . . 271
1.4 LP-Serial Protocol . . . 271
1.5 LP-Serial Registers . . . 271
1.6 Signal Descriptions . . . 271
1.7 AC Electrical Specifications . . . 271
1.8 Interface Management . . . 271

2 Chapter 2 - Packets . . . 271
2.1 Packet Field Definitions . . . 271
2.2 Packet Format . . . 272
2.3 Packet Protection . . . 272
2.3.1 Packet CRC Operation . . . 273
2.3.2 16-Bit Packet CRC Code . . . 275
2.4 Maximum Packet Size . . . 276

3 Chapter 3 - Control Symbols . . . 277
3.1 Control Symbol Field Definitions . . . 277
3.2 Control Symbol Format . . . 277
3.3 Stype0 Control Symbols . . . 278
3.3.1 Packet-Accepted Control Symbol . . . 279
3.3.2 Packet-Retry Control Symbol . . . 279
3.3.3 Packet-Not-Accepted Control Symbol . . . 279
3.3.4 Status Control Symbol . . . 280
3.3.5 Link-Response Control Symbol . . . 280
3.4 Stype1 Control Symbols . . . 282
3.4.1 Start-of-Packet Control Symbol . . . 282
3.4.2 Stomp Control Symbol . . . 283
3.4.3 End-of-Packet Control Symbol . . . 283
3.4.4 Restart-From-Retry Control Symbol . . . 283
3.4.5 Link-Request Control Symbol . . . 283
3.4.6 Multicast-Event Control Symbol . . . 284
3.5 Control Symbol Protection . . . 284
3.5.1 CRC-5 Code . . . 284
3.5.2 CRC-5 Parallel Code Generation . . . 284

4 Chapter 4 - PCS and PMA Layers 285
4.1 PCS Layer Functions 286
4.2 PMA Layer Functions. 286
4.3 Definitions 286
4.4 8B/10B Transmission Code 287
4.4.1 Character and Code-Group Notation 287
4.4.2 Running Disparity 288
4.4.3 Running Disparity Rules 288
4.4.4 8B/10B Encoding. 288
4.4.5 Transmission Order 288
4.4.6 8B/10B Decoding 289
4.4.8 Effect of Single Bit Code-Group Errors 300
4.4.9 Idle Sequence. 301
4.4.10 1x Link Transmission Rules 302
4.4.11 4x Link Striping and Transmission Rules 305
4.5 Retimers and Repeaters 306
4.5.1 Retimers. 306
4.5.2 Repeaters 307
4.6 Port Initialization 307
4.6.1 1x Mode Initialization 307
4.6.2 1x/4x Mode Initialization. 307
4.6.3 State Machines. 308

5 Chapter 5 - LP-Serial Protocol 316
5.1 Packet Exchange Protocol 316
5.2 Control Symbols 317
5.2.1 Control Symbol Delimiting 317
5.2.2 Control Symbol Transmission 318
5.2.3 Embedded Control Symbols 318
5.2.4 Multicast-Event Control Symbols 318
5.3 Packets 319
5.3.1 Packet Delimiting 319
5.3.2 Acknowledgment Identifier 319
5.3.3 Packet Priority and Transaction Request Flows 319
5.4 Link Maintenance Protocol. 320
5.5 Packet Transmission Protocol. 321
5.6 Flow Control 322
5.6.1 Receiver-Controlled Flow Control 322
5.6.2 Transmitter-Controlled Flow Control 323
5.6.3 Flow Control Mode Negotiation 326
5.7 Cancelling Packets 326
5.8 Transaction and Packet Delivery Ordering Rules. 327
5.9 Deadlock Avoidance. 327
5.10 Error Detection and Recovery 329
5.10.1 Lost Packet Detection 329
5.10.2 Link Behavior Under Error 330
5.11 Power Management 332

Table of Contents

6 Chapter 6 - LP-Serial Registers 332
6.1 Generic End Point Devices 333
6.1.1 Register Map 333
6.1.2 Command and Status Registers (CSRs) 334
6.2 Generic End Point Devices, software assisted error recovery option 338
6.2.1 Register Map 338
6.2.2 Command and Status Registers (CSRs) 339
6.3 Generic End Point Free Devices 344
6.3.1 Register Map 344
6.3.2 Command and Status Registers (CSRs) 345

7 Chapter 7 - Signal Descriptions 349
7.1 Signal Definitions 349
7.2 Serial RapidIO Interface Diagrams 350

8 Chapter 8 - AC Electrical Specifications 350
8.1 Overview 350
8.2 Signal Definition 351
8.3 Equalization 351
8.4 Explanatory Note on Transmitter and Receiver Specifications 352
8.5 Transmitter Specifications 352
8.6 Receiver Specifications 356
8.7 Receiver Eye Diagrams 357
8.8 Measurement and Test Requirements 359
8.8.1 Eye template measurements 359
8.8.2 Jitter test measurements 359
8.8.3 Transmit jitter 359
8.8.4 Jitter tolerance 359
Annex A (informative) Interface Management 360
A.1 Packet Retry Mechanism 360
A.1.1 Input port retry recovery state machine 360
A.1.2 Output port retry recovery state machine 361
A.2 Error Recovery 363
A.2.1 Input port error recovery state machine 363
A.2.2 Output port error recovery state machine 365
Annex B (informative) Critical Resource Performance Limits 367
Glossary of Terms and Abbreviations 370

VII Partition VII - Inter-operability Specification System and Device 374

1 Chapter 1 - Overview 374
1.1 Overview 374

2 Chapter 2 - System Exploration and Initialization 374
2.1 Boot code access 374
2.2 Exploration and initialization 375
2.2.1 Exploration and initialization rules 376
2.2.2 Exploration and initialization algorithm 376
2.2.3 Exploration and initialization example 376

3 Chapter 3 - RapidIO Device Class Requirements 379
3.1 Introduction 379
3.2 Class Partitioning 380
3.2.1 Generic: All devices 380
3.2.2 Class 1: Simple target device 381
3.2.3 Class 2: Simple mastering device 381
3.2.4 Class 3: Complex mastering device 381

4 Chapter 4 - PCI Considerations 382
4.1 Address Map Considerations 382
4.2 Transaction Flow 384
4.2.1 PCI 2.2 Transaction Flow 384
4.2.2 PCI-X Transaction Flow 386
4.3 RapidIO to PCI Transaction Mapping 387
4.4 Operation Ordering and Transaction Delivery 389
4.4.1 Operation Ordering 389
4.4.2 Transaction Delivery Ordering 389
4.4.3 PCI-X Relaxed Ordering Considerations 389
4.5 Interactions with Globally Shared Memory 390
4.5.1 I/O Read Operation Details 392
4.5.2 Data Cache Flush Operation Details 393
4.6 Byte Lane and Byte Enable Usage 393
4.7 Error Management 394

5 Chapter 5 - Globally Shared Memory Devices 394
5.1 Processing Element Behavior 394
5.1.1 Processor-Memory Processing Element 394
5.1.2 Memory-only Processing Element 396
5.1.3 Processor-only Processing Element 404
5.1.4 I/O Processing Element 412
5.1.5 Switch Processing Element 413
5.2 Transaction to Priority Mappings 413

Bibliography 414

Table of Contents

VIII Partition VIII - Error Management Extensions Specification 416

1 Chapter 1 - Error Management Extensions 416
1.1 Physical Layer Extensions 416
1.1.1 Port Error Detect, Enable and Capture CSRs 416
1.1.2 Error Reporting Thresholds 416
1.1.3 Error Rate Control and Status 417
1.1.4 Port Behavior When Error Rate Failed Threshold is Reached 417
1.1.5 Packet Timeout Mechanism in a Switch Device 418
1.2 Logical and Transport Layer Extensions 418
1.2.1 Logical/Transport Error Detect, Enable and Capture CSRs 419
1.2.2 Message Passing Error Detection 419
1.3 System Software Notification of Error 419
1.4 Mechanisms for Software Debug 419

2 Chapter 2 Error Management Registers 420
2.1 Additions to Existing Registers 420
2.2 New Error Management Registers 421
2.2.1 Register Map 421
2.2.2 Command and Status Registers (CSRs) 423
Annex A (informative) Error Management 431
A.1 Limitations of Error Management 431
A.2 Hot-insertion/extraction 431
A.3 Port-write 432
Glossary of Terms and Abbreviations 433

List of Figures

RapidIO Layered Hierarchy 33

Partition I - Input/Output Logical Specification

Figure 1-1. A Possible RapidIO-Based Computing System 39
Figure 1-2. Processor-Memory Processing Element Example 39
Figure 1-3. Integrated Processor-Memory Processing Element Example 40
Figure 1-4. Memory-Only Processing Element Example 40
Figure 1-5. Processor-Only Processing Element Example 40
Figure 1-6. Switch Processing Element Example 41
Figure 2-1. Read Operation 45
Figure 2-2. Write and Streaming-Write Operations 45
Figure 2-3. Write-With-Response Operation 45
Figure 2-4. Atomic (Read-Modify-Write) Operation 46
Figure 2-5. Maintenance Operation 46
Figure 2-6. Byte Alignment Example 47
Figure 2-7. Half-Word Alignment Example 47
Figure 2-8. Word Alignment Example 47
Figure 2-9. Data Alignment Example 47
Figure 3-1. Type 2 Packet Bit Stream Format 52
Figure 3-2. Type 5 Packet Bit Stream Format 53
Figure 3-3. Type 6 Packet Bit Stream Format 53
Figure 3-4. Type 8 Request Packet Bit Stream Format 54
Figure 3-5. Type 8 Response Packet Bit Stream Format 55
Figure 3-6. Type 13 Packet Bit Stream Format 56
Figure 4-1. Example Extended Features Data Structure 59

Partition II - Message Passing Logical Specification

Figure 1-1. A Possible RapidIO-Based Computing System 67
Figure 1-2. Processor-Memory Processing Element Example 67
Figure 1-3. Integrated Processor-Memory Processing Element Example 68
Figure 1-4. Memory-Only Processing Element Example 68
Figure 1-5. Processor-Only Processing Element Example 68
Figure 1-6. Switch Processing Element Example 69
Figure 2-1. Doorbell Operation 72
Figure 2-2. Message Operation 73
Figure 2-3. Byte Alignment Example 73
Figure 2-4. Half-Word Alignment Example 74
Figure 2-5. Word Alignment Example 74
Figure 3-1. Type 10 Packet Bit Stream Format 75
Figure 3-2. Type 11 Packet Bit Stream Format 76
Figure 3.3. target_info Field for Message Responses 78
Figure 3-4. Type 13 Packet Bit Stream Format 78
Figure A-1. Input port training state machine 84
Figure A-2. Output port training state machine 87
Figure A-3. Input port retry recovery state machine 89
Figure A-4. Output port retry recovery state machine 91
Figure A-5. Input port error recovery state machine 93
Figure A-6. Output port error recovery state machine 95

List of Figures

Partition III - Common Transport Specification

Figure 1-1. A Small Switch-Based System 99
Figure 1-2. A Small Ring-Based System 99
Figure 1-3. Destination-Source Transport Bit Stream 100
Figure 1-4. Maintenance Packet Transport Bit Stream 101

Partition IV - Physical Layer 8/16 LP-LVDS Specification

Figure 1-1. Example Transaction with Acknowledge 107
Figure 1-2. Packet Physical Layer Fields Format 108
Figure 1-3. Control Symbol Physical Layer Fields Format 109
Figure 1-4. Flow Control Fields Bit Stream 109
Figure 1-5. Receiver-Controlled Flow Control 114
Figure 1-6. Transmitter-Controlled Flow Control 115
Figure 1-7. Error Coverage of First 16 Bits of Packet Header 117
Figure 1-8. Naturally Aligned Packet Bit Stream 118
Figure 1-9. Naturally Aligned Packet Bit Stream Example 1 121
Figure 1-10. Naturally Aligned Packet Bit Stream Example 2 121
Figure 1-11. Padded Aligned Packet Bit Stream Example 1 121
Figure 1-12. Padded Aligned Packet Bit Stream Example 2 122
Figure 1-13. CRC Generation Pipeline 123
Figure 2-1. Framing Signal Maximum Toggle Rate for 8-bit Port 126
Figure 2-2. Framing Signal Maximum Toggle Rate for 16-bit Port 126
Figure 2-3. Control Symbol Delineation Example for 8-bit Port 126
Figure 2-4. Control Symbol Delineation Example for 16-bit Port 127
Figure 2-5. Header Marked End of Packet (8-bit Port) 128
Figure 2-6. End-Of-Packet Control Symbol Marked End of Packet (16-bit Port) 128
Figure 2-7. Pacing Idle Insertion in Packet (8-bit Port) 128
Figure 2-8. Embedded Control Symbols for 8-bit Port 129
Figure 2-9. Embedded Control Symbols for 16-bit Port 129
Figure 2-10. Request Packet Transmission Example 1 130
Figure 2-11. Request Packet Transmission Example 2 130
Figure 2-12. Request Packet Transmission Example 3 131
Figure 2-13. Request Packet Transmission Example 4 131
Figure 2-14. Response Packet Transmission Example 1 132
Figure 2-15. Response Packet Transmission Example 2 132
Figure 3-1. Type 0 Packet-Accepted Control Symbol Format 137
Figure 3-2. Type 1 Packet-Retry Control Symbol Format 138
Figure 3-3. Type 2 Packet-Not-Accepted Control Symbol Format 138
Figure 3-4. Type 4 Packet Control Symbol Format 139
Figure 3-5. Type 5 Link-Request Control Symbol Format 141
Figure 3-6. Type 6 Link-Response Control Symbol Format 141
Figure 3-7. Control Symbol Transmission Example 1 143
Figure 3-8. Control Symbol Transmission Example 2 143
Figure 5-1. Clock Distribution in a Small System 160
Figure 5-2. Clock Distribution in a Larger System 160
Figure 5-3. Clock Distribution Through the Interconnect 161

List of Figures

Figure 6-1. Routing for Equalized Skew for Several Placements 162
Figure 6-2. Potential PCB Stackups 162
Figure 6-3. Recommended device pin escape, input port, top view of device 163
Figure 6-4. Recommended device pin escape, output port, top view of device 164
Figure 6-5. Opposed orientation, same side of board 164
Figure 6-6. Opposed orientation, opposite sides of board 165
Figure 6-7. Recommended device pin escape, output port reversed, top view of device 165
Figure 6-8. Opposed orientation, output port reversed, opposite sides of board 166
Figure 7-1 RapidIO 8-bit Device to 8-bit Device Interface Diagram 168
Figure 7-2. RapidIO 8-bit Device to 16-bit Device Interface Diagram 169
Figure 7-3. RapidIO 16-bit Device to 16-bit Device Interface Diagram 169
Figure 8-1. DC driver signal levels 171
Figure 8-2. Differential Peak-Peak Voltage of Transmitter or Receiver 172
Figure 8-3. Example Compliance Mask 173
Figure 8-4. RapidIO Transmit Mask 177
Figure 8-5. Example Driver Output Eye Pattern 178
Figure 8-6. RapidIO Receive Mask 181
Figure 8-7. Example Receiver Input Eye Pattern 182
Figure 8-8. Data to Clock Skew 182
Figure 8-9. Clock to Clock Skew 183
Figure 8-10. Static Skew Diagram 184
Figure A-1. Simple Inbound Mailbox Port Structure 187
Figure A-2 Inbound Mailbox Structure 188
Figure A-3. Outbound Message Queue 189
Figure A-4. Extended Outbound Message Queue 189

Partition V - Globally Shared Memory

Figure 1-1. A Snoopy Bus-Based System 193
Figure 1-2. A Distributed Memory System 193
Figure 2-1. A Possible RapidIO-Based Computing System 195
Figure 2-2 Processor-Memory Processing Element Example 196
Figure 2-3. Integrated Processor-Memory Processing Element Example 197
Figure 2-4. Memory-Only Processing Element Example 197
Figure 2-5. Processor-Only Processing Element Example 197
Figure 2-6. Switch Processing Element Example 198
Figure 3-1. Read Operation to Remote Shared Coherence Granule 203
Figure 3-2. Read Operation to Remote Modified Coherence Granule 203
Figure 3-3. Read Operation to Local Modified Coherence Granule 203
Figure 3-4. Instruction Read Operation to Remote Shared Coherence Granule 204
Figure 3-5. Instruction Read Operation to Remote Modified Coherence Granule 204
Figure 3-6. Instruction Read Operation to Local Modified Coherence Granule 204
Figure 3-7. Instruction Read Operation Paradox Case 205
Figure 3-8. Read-for-Ownership Operation to Remote Shared Coherence Granule 205
Figure 3-9. Read-for-Ownership Operation to Remote Modified Coherence Granule 205
Figure 3-10. Read-for-Ownership Operation to Local Shared Coherence Granule 206
Figure 3-11. Read-for-Ownership Operation to Local Modified Coherence Granule 206
Figure 3-12. Data Cache Invalidate Operation to Remote Shared Coherence Granule 206

Figure 3-13. Data Cache Invalidate Operation to Local Shared Coherence Granule 207
Figure 3-14. Castout Operation on Remote Modified Coherence Granule 207
Figure 3-15. TLB Invalidate-Entry Operation 207
Figure 3-16. TLB Invalidate-Entry Synchronization Operation 208
Figure 3-17. Instruction Cache Invalidate Operation to Remote Sharable Coherence Granule 208
Figure 3-18. Instruction Cache Invalidate Operation to Local Sharable Coherence Granule 208
Figure 3-19. Flush Operation to Remote Shared Coherence Granule 209
Figure 3-20. Flush Operation to Remote Modified Coherence Granule 209
Figure 3-21. Flush Operation to Local Shared Coherence Granule 210
Figure 3-22. Flush Operation to Local Modified Coherence Granule 210
Figure 3-23. I/O Read Operation to Remote Shared Coherence Granule 210
Figure 3-24. I/O Read Operation to Remote Modified Coherence Granule 211
Figure 3-25. I/O Read Operation to Local Modified Coherence Granule 211
Figure 3-26. Byte Alignment Example 211
Figure 3-27. Half-Word Alignment Example 211
Figure 3-28. Word Alignment Example 211
Figure 3-29. Data Alignment Example 212
Figure 4-1. Type 1 Packet Bit Stream Format 217
Figure 4-2. Type 2 Packet Bit Stream Format 218
Figure 4-3. Type 5 Packet Bit Stream Format 219
Figure 4-4. Type 13 Packet Bit Stream Format 220

Partition VI - Physical Layer 1x/4x LP-Serial Specification

Figure 2-1. Packet Format 272
Figure 2.2. Packet Alignment 272
Figure 2-3. Error Coverage of First 16 Bits of Packet Header 273
Figure 2-4. Unpadded Packet of Length 80 Bytes or Less 273
Figure 2-5. Padded Packet of Length 80 Bytes or Less 274
Figure 2-6. Unpadded Packet of Length Greater than 80 Bytes 274
Figure 2-7. Padded Packet of Length Greater than 80 Bytes 274
Figure 2-8. CRC Generation Pipeline 276
Figure 3-1. Control Symbol Format 277
Figure 3-2. Packet-Accepted Control Symbol Format 279
Figure 3-3. Packet-Retry Control Symbol Format 279
Figure 3-4. Packet-Not-Accepted Control Symbol Format 280
Figure 3-5. Status Control Symbol Format 280
Figure 3-6. Link-Response Control Symbol Format 280
Figure 3-7. Start-of-Packet Control Symbol Format 282
Figure 3-8. Stomp Control Symbol Format 283
Figure 3-9. End-of-Packet Control Symbol Format 283
Figure 3-10. Restart-From-Retry Control Symbol Format 283
Figure 3-11. Link-Request Control Symbol Format 283
Figure 3-12. Multicast-Event Control Symbol Format 284
Figure 3-13. 5-bit CRC Implementation 285
Figure 4-1. Character Notation Example (D25.3) 287
Figure 4-2. Code-Group Notation Example (/D25.3/) 287

List of Figures

Figure 4-3. Lane Encoding, Serialization, Deserialization, and Decoding Process 289
Figure 4-4. Example of a Pseudo-Random Idle Code-Group Generator 302
Figure 4-5. 1x Mode Control Symbol Encoding and Transmission Order 303
Figure 4-6. 1x Mode Packet Encoding and Transmission Order 303
Figure 4-7. 1x Typical Data Flow 304
Figure 4-8. Typical 4x Data Flow 306
Figure 4-9. Lane_Synchronization State 311
Figure 4-10. Lane_Alignment State Machine 313
Figure 4-11. 1x_Initialization State Machine 314
Figure 4-12. 1x/4x_Initialization State Machine 316
Figure 5-1. Example Transaction with Acknowledgment 317
Figure 5-2. Receiver-Controlled Flow Control 323
Figure 5-3. Transmitter-Controlled Flow Control 324
Figure 7-1. RapidIO 1x Device to 1x Device Interface Diagram 350
Figure 7-2. RapidIO 4x Device to 4x Device Interface Diagram 350
Figure 7-3. RapidIO 4x Device to 1x Device Interface Diagram 350
Figure 8-1. Differential Peak-Peak Voltage of Transmitter or Receiver 351
Figure 8-2. Transmitter Output Compliance Mask 355
Figure 8-3. Single Frequency Sinusoidal Jitter Limits 358
Figure 8-4. Receiver Input Compliance Mask 358
Figure A-1. Input Port Retry Recovery State Machine 360
Figure A-2. Output Port Retry Recovery State Machine 362
Figure A-3. Input Port Error Recovery State Machine 364
Figure A-4. Output Port Error Recovery State Machine 365

Partition VII - Interoperability Specification System and Device

Figure 1-1. RapidIO Documentation Hierarchy 374
Figure 2-1. Example system with boot ROM 375
Figure 2-2. Automatically finding the boot ROM 375
Figure 2-3. Example system 377
Figure 2-4. Finding the adjacent device 377
Figure 2-5. Finding the device on switch port 0 378
Figure 2-6. Finding the device on switch port 1 378
Figure 2-7. Finding the device on switch port 3 379
Figure 2-8. Final initialized system state 379
Figure 4-1. Example System with PCI and RapidIO 382
Figure 4-2. Host segment PCI Memory Map Example 383
Figure 4-3. AMT and Memory Mapping 384
Figure 4-4. PCI Mastered Posted Write Transaction Flow Diagram 384
Figure 4-5. PCI Mastered non-posted (delayed) Transaction Flow Diagram 385
Figure 4-6. RapidIO Mastered Transaction 386
Figure 4-7. PCI-X Mastered Split Response Transaction 387
Figure 4-8. Traditional Non-coherent I/O Access Example 390
Figure 4-9. Traditional Globally Coherent I/O Access Example 391
Figure 4-10. RapidIO Locally Coherent I/O Access Example 392

Partition VIII - Error Management Extentions Specification

List of Tables

Partition I - Input/Output Logical Specification

Table 2-1. I/O Operations Cross Reference 44
Table 3-1. Request Packet Type to Transaction Type Cross Reference 48
Table 3-2. General Field Definitions for All Request Packets 49
Table 3-3. Read Size (rdsize) Definitions 49
Table 3-4. Write Size (wrsize) Definitions 50
Table 3-5. Transaction Fields and Encodings for Type 2 Packets 51
Table 3-6. Transaction Fields and Encodings for Type 5 Packets 52
Table 3-7. Specific Field Definitions and Encodings for Type 8 Packets 54
Table 3-8. Response Packet Type to Transaction Type Cross Reference 55
Table 3-9. Field Definitions and Encodings for All Response Packets 56
Table 4-1. I/O Register Map 57
Table 4-2. Configuration Space Reserved Access Behavior 58
Table 4-3. Bit Settings for Device Identity CAR 59
Table 4-4. Bit Settings for Device Information CAR 59
Table 4-5. Bit Settings for Assembly Identity CAR 60
Table 4-6. Bit Settings for Assembly Information CAR 60
Table 4-7. Bit Settings for Processing Element Features CAR 60
Table 4-8. Bit Settings for Switch Port Information CAR 61
Table 4-9. Bit Settings for Source Operations CAR 61
Table 4-10. Bit Settings for Destination Operations CAR 62
Table 4-11. Bit Settings for Write Port CSR 62
Table 4-12. Bit Settings for Processing Element Logical Layer Control CSR 63
Table 4-13. Bit Settings for Local Configuration Space Base Address 0 CSR 63
Table 4-14. Bit Settings for Local Configuration Space Base Address 1 CSR 64

Partition II - Message Passing Logical Specification

Table 2-1. Message Passing Operations Cross Reference 72
Table 3-1. Request Packet Type to Transaction Type Cross Reference 74
Table 3-2. General Field Definitions for All Request Packets 75
Table 3-3. Specific Field Definitions for Type 10 Packets 75
Table 3-4. Specific Field Definitions and Encodings for Type 11 Packets 75
Table 3-5. Response Packet Type to Transaction Type Cross Reference 77
Table 3-6. Field Definitions and Encodings for All Response Packets 77
Table 3-7. Specific Field Definitions for Type 13 Packets 78
Table 4-1. Message Passing Register Map 79
Table 4-2. Configuration Space Reserved Access Behavior 79
Table 4-3. Bit Settings for Processing Element Features CAR 80
Table 4-4. Bit Settings for Source Operations CAR 81
Table 4-5. Bit Settings for Destination Operations CAR 81
Table 4-6. Bit Settings for Mailbox CSR 81
Table 4-7. Bit Settings for Doorbell CSR 83
Table A-1. Input port training state machine transition table 85
Table A-2. Output port training state machine transition table 87
Table A-3. Input port retry recovery state machine transition table 90
Table A-4. Output port retry recovery state machine transition table 91
Table A-5. Input port error recovery state machine transition table 93
Table A-6. Output port error recovery state machine transition table 95

Partition III - Common Transport Specification

Table 1-1. tt Field Definition . . . 100
Table 2-1. Common Transport Register Map . . . 101
Table 2-2. Configuration Space Reserved Access Behavior . . . 102
Table 2-3. Bit Settings for Processing Element Features CAR . . . 103
Table 2-4. Bit Settings for Base Device ID CSR . . . 103
Table 2-5. Bit Settings for Host Base Device ID Lock CSR . . . 104
Table 2-6. Bit Settings for Component ID CSR . . . 104

Partition IV - Physical Layer 8/16 LP-LVDS Specification

Table 1-1. Fields that Control Packet Flow . . . 108
Table 1-2. buf_status Field Definition . . . 109
Table 1-3. Transaction Request Flow to Priority Mapping . . . 110
Table 1-4. Parallel CRC Intermediate Value Equations . . . 122
Table 1-5. Secondary Link Maintenance Command Summary . . . 124
Table 1-6. Link Status Indicators . . . 125
Table 3-1. Field Definitions for Acknowledgment Control Symbols . . . 137
Table 3-2. Cause Field Definition . . . 138
Table 3-3. sub_type and contents Field Definitions . . . 139
Table 3-4. Throttle Control Symbol contents Field Definition . . . 140
Table 3-5. cmd Field Definition . . . 141
Table 3-6. ackID_status Field Definition . . . 141
Table 3-7. link_status Field Definition . . . 142
Table 4-1. Extenended Feature Space Reserved Access Behaviour . . . 144
Table 4-2. Physical 8/16 LP-LVDS Register Map . . . 144
Table 4-3. Bit Settings for Port Maintenance Block Header 0 . . . 145
Table 4-4. Bit Settings for Port Maintenance Block Header 1 . . . 145
Table 4-5. Bit Settings for Port Link Time-out Control CSR . . . 145
Table 4-6. Bit Settings for Port Response Time-out Control CSR . . . 146
Table 4-7. Bit Settings for Port General Control CSRs . . . 146
Table 4-8. Bit Settings for Port n Error and Status CSRs . . . 147
Table 4-9. Bit Settings for Port n Control CSRs . . . 148
Table 4-10. Physical 8/16 LP-LVDS Register Map . . . 149
Table 4-11. Bit Settings for Port Maintenance Block Header 0 . . . 150
Table 4-12. Bit Settings for Port Maintenance Block Header 1 . . . 150
Table 4-13. Bit Settings for Port Link Time-out Control CSR . . . 150
Table 4-14. Bit Settings for Port Response Time-out Control CSR . . . 150
Table 4-15. Bit Settings for Port General Control CSRs . . . 151
Table 4-16. Bit Settings for Port n Link Maintenance Request CSRs . . . 151
Table 4-17. Bit Settings for Port n Link Maintenance Response CSRs . . . 151
Table 4-18. Bit Settings for Port n Local ackID Status CSRs . . . 153
Table 4-19. Bit Settings for Port n Error and Status CSRs . . . 153
Table 4-20. Bit Settings for Port n Control CSRs . . . 154
Table 4-21. Physical 8/16 LP-LVDS Register Map . . . 156
Table 4-22. Bit Settings for Port Maintenance Block Header 0 . . . 156
Table 4-23. Bit Settings for Port Maintenance Block Header 1 . . . 157

Table 4-24. Bit Settings for Port Link Time-out Control CSR 157
Table 4-25. Bit Settings for Port General Control CSRs 157
Table 4-26. Bit Settings for Port n Error and Status CSRs 157
Table 4-27 Bit Settings for Port n Control CSRs 158
Table 7-1. Memory Interface Signal Description 166
Table 8-1. RapidIO 8/16 LP-LVDS Driver Specifications (DC) 170
Table 8-2. RapidIO 8/16 LP-LVDS Receiver Specifications (DC) 171
Table 8-3. Driver AC Timing Specifications - 500Mbps Data Rate/250MHz Clock Rate 174
Table 8-4. Driver AC Timing Specifications - 750Mbps Data Rate/375MHz Clock Rate 174
Table 8-5. Driver AC Timing Specifications - 1000Mbps Data Rate/500MHz Clock Rate 175
Table 8-6. Driver AC Timing Specifications - 1500Mbps Data Rate/750MHz Clock Rate 176
Table 8-7. Driver AC Timing Specifications - 2000Mbps Data Rate/1000MHz Clock Rate 176
Table 8-8. Receiver AC Timing Specifications - 500Mbps Data Rate/250MHz Clock Rate 179
Table 8-9. Receiver AC Timing Specifications - 750Mbps Data Rate/375MHz Clock Rate 179
Table 8-10. Receiver AC Timing Specifications - 1000Mbps Data Rate/500MHz Clock Rate 179
Table 8-11. Receiver AC Timing Specifications - 1500Mbps Data Rate/750MHz Clock Rate 180
Table 8-12. Receiver AC Timing Specifications - 2000Mbps Data Rate/1000MHz Clock Rate 180

Partition V - Globally Shared Memory

Table 2-1. RapidIO Memory Directory Definition 199
Table 3-1. GSM Operations Cross Reference 201
Table 4-1. Request Packet Type to Transaction Type Cross Reference 212
Table 4-2. Coherent 32-Byte Read Data Return Ordering 214
Table 4-3. Coherent 64-Byte Read Data Return Ordering 214
Table 4-4. General Field Definitions for All Request Packets 214
Table 4-5. Read Size (rdsize) Definitions 215
Table 4-6. Write Size (wrsize) Definitions 216
Table 4-7. Specific Field Definitions and Encodings for Type 1 Packets 217
Table 4-8. Transaction Field Encodings for Type 2 Packets 218
Table 4-9. Transaction Field Encodings for Type 5 Packets 219
Table 4-10. Request Packet Type to Transaction Type Cross Reference 219
Table 4-11. Field Definitions and Encodings for All Response Packets 220
Table 5-1. GSM Register Map 221
Table 5-2. Configuration Space Reserved Access Behavior 222
Table 5-3. Bit Settings for Source Operations CAR 223
Table 5-4. Bit Settings for Destination Operations CAR 223
Table 6-1. Operation to Protocol Cross Reference 226
Table 7-1. Address Collision Resolution for READ_HOME 248
Table 7-2. Address Collision Resolution for IREAD_HOME 249
Table 7-3. Address Collision Resolution for READ_OWNER 250
Table 7-4. Address Collision Resolution for READ_TO_OWN_HOME 250
Table 7-5. Address Collision Resolution for READ_TO_OWN_OWNER 252
Table 7-6. Address Collision Resolution for DKILL_HOME 253
Table 7-7. Address Collision Resolution for DKILL_SHARER 254
Table 7-8. Address Collision Resolution for IKILL_HOME 255
Table 7-9. Address Collision Resolution for IKILL_SHARER 256

Table 7-10. Address Collision Resolution for CASTOUT 257
Table 7-11. Address Collision Resolution for Software Coherence Operations 258
Table 7-12. Address Collision Resolution for Participant FLUSH 258
Table 7-13. Address Collision Resolution for Non-participant FLUSH 259
Table 7-14. Address Collision Resolution for Participant IO_READ_HOME 260
Table 7-15. Address Collision Resolution for Non-participant IO_READ_HOME 261
Table 7-16. Address Collision Resolution for Participant IO_READ_OWNER 262
Table 7-17. Address Collision Resolution for Non-participant IO_READ_OWNER 263

Partition VI - Physical Layer 1x/4x LP-Serial Specification

Table 2.1 - Packet Field Definitions 272
Table 2-2. Parallel CRC Intermediate Value Equations 275
Table 2-3. Maximum Packet Size 276
Table 3-1. Control Symbol Field Definitions 277
Table 3-2. Stype0 Control Symbol Encoding 278
Table 3-3. Stype0 Parameter Definitions 279
Table 3-4. Cause Field Definition 280
Table 3-5. Port_status Field Definitions 281
Table 3-6. Stype1 Control Symbol Encoding 282
Table 3-7. Cmd Field Definitions 283
Table 3-8. Parallel CRC Equations 285
Table 4-1. Data Character Encodings 289
Table 4-2. Special Character Encodings 298
Table 4-3. Special Characters and Columns 299
Table 4-4. Code-Group Corruption Caused by Single Bit Errors 300
Table 5-1. Transaction Request Flow to Priority Mapping 320
Table 6-1. Extended Feature Space Reserved Access Behavior 333
Table 6-2. LP-Serial Register Map - Generic End Point Device 333
Table 6-3. Bit Settings for Port Maintenance Block Header 0 334
Table 6-4. Bit Settings for Port Maintenance Block Header 1 335
Table 6-5. Bit Settings for Port Link Time-out Control CSR 335
Table 6-6. Bit Settings for Port Response Time-out Control CSR 335
Table 6-7. Bit Settings for Port General Control CSRs 335
Table 6-8. Bit Settings for Port n Error and Status CSRs 336
Table 6-9. Bit Settings for Port n Control CSRs 337
Table 6-10. LP-Serial Register Map - Generic End Point Devices (SW assisted) 338
Table 6-11. Bit Settings for Port Maintenance Block Header 0 339
Table 6-12. Bit Settings for Port Maintenance Block Header 1 340
Table 6-13. Bit Settings for Port Link Time-out Control CSR 340
Table 6-14. Bit Settings for Port Response Time-out Control CSR 340
Table 6-15. Bit Settings for Port General Control CSRs 340
Table 6-16. Bit Settings for Port n Link Maintenance Request CSRs 341
Table 6-17. Bit Settings for Port n Link Maintenance Response CSRs 341
Table 6-18. Bit Settings for Port n Local ackID Status CSRs 341
Table 6-19. Bit Settings for Port n Error and Status CSRs 342
Table 6-20. Bit Settings for Port n Control CSRs 343

List of Tables

Table 6-21. LP-Serial Register Map - Generic End Point Free 344
Table 6-22. Bit Settings for Port Maintenance Block Header 0 345
Table 6-23. Bit Settings for Port Maintenance Block Header 1 346
Table 6-24. Bit Settings for Port Link Time-out Control CSR 346
Table 6-25. Bit Settings for Port General Control CSRs 346
Table 6-26. Bit Settings for Port n Error and Status CSRs 346
Table 6-27. Bit Settings for Port n Control CSRs 348
Table 7-1. 1x/4x LP-Serial Signal Description 349
Table 8-1. Short Run Transmitter AC Timing Specifications - 1.25 Gbps 352
Table 8-2. Short Run Transmitter AC Timing Specifications - 2.5 Gbps 353
Table 8-3. Short Run Transmitter AC Timing Specifications - 3.125 Gbps 353
Table 8-4. Long Run Transmitter AC Timing Specifications - 1.25 Gbps 354
Table 8-5. Long Run Transmitter AC Timing Specifications - 2.5 Gbps 354
Table 8-6. Long Run Transmitter AC Timing Specifications - 3.125 Gbps 355
Table 8-7. Transmitter Differential Output Eye Diagram Parameters 356
Table 8-8. Receiver AC Timing Specifications - 1.25 Gbps 356
Table 8-9. Receiver AC Timing Specifications - 2.5 Gbps 357
Table 8-10. Receiver AC Timing Specifications - 3.125 Gbps 357
Table 8-11. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter 359
Table A-1. Input Port Retry Recovery State Machine Transition Table 361
Table A-2. Output Port Retry Recovery State Machine Transition Table 362
Table A-3. Input Port Error Recovery State Machine Transition 364
Table A-4. Output Port Error Recovery State Machine Transition 365
Table B-1. Packet Transmission Delay Components 367
Table B-2. Packet Acknowledgment Delay Components 368
Table B-3. Packet Delays 369
Table B-4. Maximum Transmission Distances 369

Partition VII - Interoperability Specification System and Device

Table 4-1. PCI 2.2 to RapidIO Transaction Mapping 387
Table 4-2. PCI-X to RapidIO Transaction Mapping 388
Table 4-3. Packet priority assignments for PCI ordering 389
Table 4-4. Packet priority assignments for PCI-X ordering 390
Table 7-1. Transaction to Priority Mapping 414

Partition VIII - Error Management Extentions Specification

Table 1-1. Port Behavior when Error Rate Failed Threshold has been hit 418
Table 1-2. Port-write Packet Data Payload for Error Reporting 419
Table 2-1. Bit Settings for Port n Control CSRs 420
Table 2-2. Bit Settings for Port n Error and Status CSRs 421
Table 2-3. Extended Feature Space Reserved Access Behavior 421
Table 2-4. Error Reporting Register Map 422
Table 2-5. Bit Settings for Port Maintenance Block Header 423
Table 2-6. Bit Settings for Logical/Transport Layer Error Detect CSR 423
Table 2-7. Bit Settings for Logical/Transport Layer Error Enable CSR 424
Table 2-8. Bit Settings for Logical/Transport Layer High Address Capture CSR 425
Table 2-9. Bit Settings for Logical/Transport Layer Address Capture CSR 425

List of Tables

Table 2-10. Bit Settings for Logical/Transport Layer Device ID Capture CSR 426
Table 2-11. Bit Settings for Logical/Transport Layer Header Capture CSR 1 426
Table 2-12. Bit Settings for Port-write Target deviceID CSR 426
Table 2-13. Bit Settings for Packet Time-to-live CSR 426
Table 2-14. Bit Settings for Port n Error Detect CSR 427
Table 2-15. Bit Settings for Port n Error Rate Enable CSR 427
Table 2-16. Bit Settings for Port n Attributes Error Capture CSR 428
Table 2-17. Bit Settings for Port n Packet/Control Symbol Error Capture CSR 0 429
Table 2-18. Bit Settings for Port n Packet Error Capture CSR 1 429
Table 2-19. Bit Settings for Port n Packet Error Capture CSR 2 429
Table 2-20. Bit Settings for Port n Packet Error Capture CSR 3 429
Table 2-21. Bit Settings for Port n Error Rate CSR 430
Table 2-22. Bit Settings for Port n Error Rate Threshold CSR 430