

ISO/IEC 11518-10:2001-03 (E)

Information technology_ - High-performance parallel interface_ - Part_10: 6400_Mbit/s Physical Layer_(HIPPI-6400-PH)

CONTENTS

- FOREWORD 6
- INTRODUCTION 7

- 1 Scope 8
- 2 Normative references 8
- 3 Definitions and conventions 9
 - 3.1 Definitions 9
 - 3.2 Editorial conventions 10
 - 3.3 Acronyms and abbreviations 11
- 4 System overview 11
 - 4.1 Overview 11
 - 4.2 Links 12
 - 4.3 Virtual Channels 12
 - 4.4 Micropacket 13
 - 4.5 Message 14
 - 4.6 FRAME and CLOCK signals 15
 - 4.7 Flow control 15
 - 4.8 Retransmission 15
 - 4.9 Check functions 15
 - 4.10 Local electrical interface (optional) 15
 - 4.11 Copper cable physical layer (optional) 16
- 5 Service interface 16
 - 5.1 Overview 16
 - 5.2 Service primitives 17
 - 5.3 Sequences of primitives 17
 - 5.4 Data transfer service primitives 17
 - 5.5 Admin service primitives 20
 - 5.6 Control service primitives 22
 - 5.7 Status service primitives 23
- 6 Micropacket contents 24
 - 6.1 Bit and byte assignments 24
 - 6.2 Virtual Channel (VC) selector 26
 - 6.3 Micropacket TYPEs 26
 - 6.4 Sequence number parameters 27
 - 6.5 Credit update parameters 28
 - 6.6 Check functions 28
- 7 Message structure 31
 - 7.1 Overview 31
 - 7.2 MAC header 31
 - 7.3 LLC/SNAP header 32
 - 7.4 Payload 32

8	Source specific operations	32
8.1	Credit update indications on Source side	32
8.2	ACK indications on Source side	32
8.3	ACKs and credit updates to remote end	33
8.4	Micropacket retransmission	33
9	Destination specific operations	34
9.1	Link level processing	34
9.2	Check for Message protocol errors	34
9.3	Generating ACKs	36
10	Signal line encoding	36
10.1	Signal line bit assignments	36
10.2	CLOCK and CLOCK_2 signals	36
10.3	FRAME signal	39
10.4	Source-side encoding for d.c. balance	39
10.5	Destination-side decoding	41
11	Skew compensation	41
11.1	Training sequences	41
11.2	Training sequence errors	42
12	Link Reset and Initialization	42
12.1	Overview	42
12.2	Link Reset	43
12.3	Initialize	43
12.4	Hold-off timer	45
13	Link activity monitoring and shutdown	45
13.1	Activity monitoring	45
13.2	Link shutdown	45
14	Maintenance and control features	46
14.1	Timeouts	46
14.2	Logged events	46
15	Local electrical interface (optional)	47
15.1	Overview	47
15.2	Local electrical interface – Output	49
15.3	Local electrical interface – Input	49
15.4	Light present signal	49
16	Copper cable interface (optional)	51
16.1	Overview	51
16.2	Copper cable interface – Output	51
16.3	Copper cable interface – Input	52
16.4	CLOCK_2	53
16.5	Copper cable connectors	54
16.6	Copper cable specifications	55
	Annex A (informative) Implementation comments	61

Figure 1 – System overview	12
Figure 2 – HIPPI-6400-PH link showing signal lines	13
Figure 3 – Logical micropacket format and naming conventions	14
Figure 4 – Message format.....	14
Figure 5 – Reverse direction control information.....	16
Figure 6 – HIPPI-6400-PH service interface	17
Figure 7 – Data transfer service primitives	18
Figure 8 – Admin service primitives	20
Figure 9 – Control service primitives	22
Figure 10 – Status service primitives.....	23
Figure 11 – Control bits summary.....	25
Figure 12 – LCRC implementation example.....	30
Figure 13 – ECRC implementation example	30
Figure 14 – Header micropacket contents	31
Figure 15 – Detailed ULA layout.....	32
Figure 16 – 16-bit system micropacket	40
Figure 17 – 8-bit system micropacket	41
Figure 18 – 16-bit system training sequence	41
Figure 19 – 8-bit system training sequence	42
Figure 20 – Initialize and Link Reset sequences.....	44
Figure 21 – Local electrical interface block diagram	48
Figure 22 – One signal (of 12 in each direction) of the local electrical interface.....	49
Figure 23 – One signal (of 23 in each direction) of the copper cable interface	52
Figure 24 – Destination Receiver equivalent circuit	52
Figure 25 – Receiver eye mask (differential)	54
Figure 26 – Connecting the overall shield.....	55
Figure 27 – Receptacle pin assignments	57
Figure 28 – Receptacle	59
Figure 29 – Cable connector	60
Figure A.1 – Encode / decode circuit example	61
Figure A.2 – Parallel LCRC generator example	62
Figure A.3 – Parallel LCRC checker example	63
Figure A.4 – Parallel ECRC example.....	64
Table 1 – CRC coverages in a 128-byte Message	16
Table 2 – Micropacket contents summary.....	28
Table 3 – Signal line bit assignments in a 16-bit system	37
Table 4 – Signal line bit assignments in an 8-bit system.....	38
Table 5 – 4b/5b line coding	40
Table 6 – Summary of timeouts	46
Table 7 – Summary of logged events.....	47
Table 8 – Local electrical signal timing at Source driver output.....	50

Table 9 – Local electrical interface, Source driver output.....	50
Table 10 – Local electrical interface, Destination receiver input.....	51
Table 11 – Copper cable interface.....	51
Table 12 – Copper cable interface signal timing at Source driver output.....	53
Table 13 – Copper cable interface, Source driver output	53
Table 14 – Copper cable interface, Destination receiver input	54
Table 15 – Copper cable assembly electrical specifications.....	56
Table 16 – Cable layout	58
Table A.1 – Parallel LCRC input bits	62
Table A.2 – Parallel ECRC input bits	63
Table A.3 – 16-bit LCRC generator equations	65
Table A.4 – 64-bit LCRC generator equations	66
Table A.5 – 80-bit LCRC checker equations	67
Table A.6 – 64-bit ECRC generator / checker equations.....	68