

ISO/IEC 24739-2:2009-11 (E)

Information technology_ - AT Attachment with Packet Interface_ - 7_ - Part_2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)

CONTENTS

FOREWORD.....	10
INTRODUCTION.....	11
1 Scope.....	12
2 Normative references.....	12
3 Terms, definitions, abbreviations, conventions and keywords	12
3.1 Terms, definitions and abbreviations.....	12
3.2 Abbreviations.....	21
3.3 Conventions	22
3.3.1 General	22
3.3.2 Precedence	22
3.3.3 Lists	22
3.3.4 Keywords.....	22
3.3.5 Numbering.....	23
3.3.6 Signal conventions.....	24
3.3.7 Bit conventions	24
3.3.8 State diagram conventions.....	25
3.3.9 Timing conventions.....	26
3.3.10 Byte ordering for data transfers.....	26
3.3.11 Byte, word and DWORD relationships	28
3.4 Relationship of this part of ISO/IEC 24739 to ISO/IEC 24739-1 and ISO/IEC 24739-3	28
4 General operational requirements	28
5 I/O register descriptions	28
6 Command descriptions	28
7 Parallel interface physical and electrical requirements.....	29
7.1 Cable configuration.....	29
7.2 Electrical characteristics	29
7.2.1 General	29
7.2.2 AC characteristics measurement techniques	31
7.2.3 Driver types and required termination.....	32
7.2.4 Electrical characteristics for Ultra DMA	32
7.3 Connectors and cable assemblies.....	35
7.3.1 General	35
7.3.2 40-pin connector.....	35
7.3.3 4-pin power connector.....	44
7.3.4 Unitized connectors	46
7.3.5 50-pin 65 mm (2.5 in) form factor style connector.....	48
7.3.6 68-pin PCMCIA connector.....	51
7.3.7 48 mm (1.8 in) 3.3 V parallel connector	54
7.4 Physical form factors	57
7.4.1 95 mm (3.5 in) form factor.....	57
7.4.2 65 mm (2.5 in) form factor.....	59
7.4.3 48 mm (1.8 in) PCMCIA form factor	64
7.4.4 48 mm (1.8 in) 5 V parallel form factor	64
7.4.5 48 mm (1.8 in) 3.3 V parallel form factor	68
7.4.6 130 mm (5.25 in) form factor.....	69

8	Parallel interface signal assignments and descriptions	73
8.1	Signal summary	73
8.2	Signal descriptions	74
8.2.1	CS(1:0)- (Chip select)	74
8.2.2	DA(2:0) (Device address).....	74
8.2.3	DASP- (device active, device 1 present).....	74
8.2.4	DD(15:0) (Device data)	74
8.2.5	DIOR-:HDMARDY-:HSTROBE (Device I/O read:Ultra DMA ready:Ultra DMA data strobe).....	74
8.2.6	DIOW-:STOP (Device I/O write:Stop Ultra DMA burst).....	74
8.2.7	DMACK- (DMA acknowledge).....	75
8.2.8	DMARQ (DMA request).....	75
8.2.9	INTRQ (Device interrupt)	75
8.2.10	IORDY:DDMARDY-:DSTROBE (I/O channel ready:Ultra DMA ready:Ultra DMA data strobe).....	75
8.2.11	PDIAG-:CBLID- (passed diagnostics: cable assembly type identifier)	76
8.2.12	RESET- (Hardware reset)	77
8.2.13	CSEL (cable select)	78
9	Parallel interface general operational requirements of the physical, data link and transport layers.....	79
9.1	Interrupts.....	79
9.2	Multiword DMA	80
9.3	Ultra DMA feature set	81
9.3.1	Overview	81
9.3.2	Phases of operation	82
9.4	Host determination of cable type by detecting CBLID-	83
10	Parallel interface register addressing	86
11	Parallel interface transport protocol.....	93
11.1	General	93
11.2	Power-on and hardware reset protocol	96
11.3	Software reset protocol	100
11.4	Bus idle protocol	105
11.5	Non-data command protocol	116
11.6	PIO data-in command protocol	118
11.7	PIO data-out command protocol.....	122
11.8	DMA command protocol.....	126
11.9	PACKET command protocol.....	129
11.10	READ/WRITE DMA QUEUED command protocol	141
11.11	EXECUTE DEVICE DIAGNOSTIC command protocol.....	145
11.12	DEVICE RESET command protocol.....	150
11.13	Ultra DMA data-in commands.....	152
11.13.1	Initiating an Ultra DMA data-in burst	152
11.13.2	The data-in transfer.....	152
11.13.3	Pausing an Ultra DMA data-in burst.....	152
11.14	Ultra DMA data-out commands.....	155
11.14.1	Initiating an Ultra DMA data-out burst	155
11.14.2	Data-out transfer	155
11.14.3	Pausing an Ultra DMA data-out burst.....	155
11.14.4	Terminating an Ultra DMA data-out burst.....	156

11.15	Ultra DMA CRC rules	157
12	Parallel interface timing	159
12.1	Deskewing.....	159
12.2	Transfer timing	159
12.2.1	General	159
12.2.2	Register transfers	159
12.2.3	PIO data transfers	161
12.2.4	Multiword DMA data transfer	164
12.2.5	Ultra DMA data transfer	168
13	Serial interface overview	182
14	Serial interface physical layer.....	182
15	Serial interface link layer.....	182
16	Serial interface transport layer	182
17	Serial interface device command layer	182
18	Host command layer	182
19	Serial interface host adapter register interface	182
20	Serial interface error handling	182
Annex A (informative)	Command Set summary	183
Annex B (informative)	Design and programming considerations for large physical sector sizes.....	184
Annex C (informative)	Device determination of cable type.....	185
C.1	Overview	185
C.2	Sequence for device detection of installed capacitor.....	185
C.3	Using the combination of methods for detecting cable type.....	187
Annex D (informative)	Signal integrity and UDMA guide	188
D.1	General	188
D.2	Issues	188
D.2.1	General	188
D.2.2	Timing	189
D.2.3	Crosstalk	195
D.2.4	Ground/power bounce.....	207
D.2.5	Ringling and data settling time (DST) for the 40-conductor cable assembly	208
D.3	System guidelines for Ultra DMA.....	214
D.3.1	General	214
D.3.2	System capacitance.....	214
D.3.3	Pull-up and pull-down resistors	214
D.3.4	Cables and connectors	214
D.3.5	Host PCB and IC design	215
D.3.6	Sender and recipient component I/Os	215
D.4	Ultra DMA electrical characteristics.....	216
D.4.1	General	216
D.4.2	DC characteristics	216
D.4.3	AC characteristics	218
D.5	Ultra DMA timing and protocol.....	218
D.5.1	Ultra DMA timing assumptions	218
D.5.2	Ultra DMA timing parameters	221
D.5.3	Ultra DMA protocol considerations	233

D.6 Cable detection.....	238
D.6.1 General	238
D.6.2 80-conductor cable assembly electrical feature	238
D.6.3 Host determination of cable assembly type.....	238
D.6.4 Device determination of cable assembly type	239
Annex E (informative) Register selection address summary	242
Annex F (informative) Sample Code for CRC and Scrambling	244
Annex G (informative) FIS type field value selection	245
Annex H (informative) Physical Layer Implementation Examples	246
Annex I (informative) Command processing Example	247
Bibliography	248
Figure 1 – ATA document relationships	11
Figure 2 – State diagram convention	25
Figure 3 – Byte, word and DWORD relationships	28
Figure 4 – Ultra DMA termination with pull-up or pull-down	34
Figure 5 – Host or device 40-pin I/O header.....	36
Figure 6 – 40-pin I/O cable connector	37
Figure 7 – 40-pin I/O header mounting	38
Figure 8 – 40-conductor cable configuration	39
Figure 9 – 80-conductor ribbon cable.....	40
Figure 10 – 80-conductor cable configuration	41
Figure 11 – Connector labeling for even or odd conductor grounding	44
Figure 12 – Device 4-pin power header	44
Figure 13 – 4-pin power cable connector	45
Figure 14 – Unitized connector	47
Figure 15 – Unitized connector	48
Figure 16 – 50-pin 65 mm (2.5 in) form factor style connector.....	49
Figure 17 – 48 mm (1.8 in) 3.3 V parallel connector	54
Figure 18 – 48 mm (1.8 in) 3.3 V parallel host connector	55
Figure 19 – 95 mm (3.5 in) form factor	58
Figure 20 – 65 mm (2.5 in) form factor	60
Figure 21 – 65 mm (2.5 in) form factor mounting holes	62
Figure 22 – 65 mm (2.5 in) form factor connector location	63
Figure 23 – 48 mm (1.8 in) 5 V parallel form factor	65
Figure 24 – 48 mm (1.8 in) 5 V parallel form factor connector location	67
Figure 25 – 48 mm (1.8 in) 3.3 V parallel form factor	68
Figure 26 – 130 mm (5.25 in) HDD form factor	70
Figure 27 – 130 mm (5.25 in) CD-ROM form factor.....	71
Figure 28 – 130 mm (5.25 in) CD-ROM connector location.....	72
Figure 29 – Cable select example.....	78
Figure 30 – Alternate cable select example	79
Figure 31 – Example configuration of a system with a 40-conductor cable.....	84

Figure 32 – Example configuration of a system where the host detects a 40-conductor cable.....	84
Figure 33 – Example configuration of a system where the host detects an 80-conductor cable.....	85
Figure 34 – Overall host protocol state sequence	94
Figure 35 – Overall device protocol state sequence	95
Figure 36 – Host power-on or hardware reset state diagram	96
Figure 37 – Device power-on or hardware reset state diagram	97
Figure 38 – Host software reset state diagram.....	101
Figure 39 – Device 0 software reset state diagram.....	102
Figure 40 – Device 1 software reset state diagram.....	104
Figure 41 – Host bus idle state diagram.....	106
Figure 42 – Additional Host bus idle state diagram with overlap or overlap and queuing	108
Figure 43 – Device bus idle state diagram	111
Figure 44 – Additional device bus idle state diagram with overlap or overlap and queuing.....	113
Figure 45 – Host non-data state diagram	117
Figure 46 – Device non-data state diagram.....	117
Figure 47 – Host PIO data-in state diagram	119
Figure 48 – Device PIO data-in state diagram.....	121
Figure 49 – Host PIO data-out state diagram	123
Figure 50 – Device PIO data-out state diagram.....	125
Figure 51 – Host DMA state diagram	127
Figure 52 – Device DMA state diagram.....	128
Figure 53 – Host PACKET non-data and PIO data command state diagram	130
Figure 54 – Device PACKET non-data and PIO data command state diagram	133
Figure 55 – Host PACKET DMA command state diagram.....	136
Figure 56 – Device PACKET DMA command state diagram	139
Figure 57 – Host DMA QUEUED state diagram.....	142
Figure 58 – Device DMA QUEUED command state diagram	144
Figure 59 – Host EXECUTE DEVICE DIAGNOSTIC state diagram	146
Figure 60 – Device 0 EXECUTE DEVICE DIAGNOSTIC state diagram.....	147
Figure 61 – Device 1 EXECUTE DEVICE DIAGNOSTIC command state diagram.....	149
Figure 62 – Host DEVICE RESET command state diagram.....	150
Figure 63 – Device DEVICE RESET command state diagram	151
Figure 64 – Example parallel CRC generator	158
Figure 65 – Register transfer to/from device	160
Figure 66 – PIO data transfer to/from device	162
Figure 67 – Initiating a multiword DMA data burst.....	165
Figure 68 – Sustaining a multiword DMA data burst.....	166
Figure 69 – Device terminating a Multiword DMA data burst.....	167
Figure 70 – Host terminating a multiword DMA data burst.....	168
Figure 71 – Initiating an Ultra DMA data-in burst.....	172
Figure 72 – Sustained Ultra DMA data-in burst	173

Figure 73 – Host pausing an Ultra DMA data-in burst.....	174
Figure 74 – Device terminating an Ultra DMA data-in burst	175
Figure 75 – Host terminating an Ultra DMA data-in burst.....	176
Figure 76 – Initiating an Ultra DMA data-out burst.....	177
Figure 77 – Sustained Ultra DMA data-out burst	178
Figure 78 – Device pausing an Ultra DMA data-out burst	179
Figure 79 – Host terminating an Ultra DMA data-out burst	180
Figure 80 – Device terminating an Ultra DMA data-out burst	181
Figure C.1 – Example configuration of a system where the device detects a 40-conductor cable.....	186
Figure D.1 – A transmission line with perfect source termination.....	190
Figure D.2 – Waveforms on a source-terminated bus with rise time less than T_{prop}	190
Figure D.3 – Waveforms on a source-terminated bus with rise time greater than T_{prop}	191
Figure D.4 – Waveforms on a source-terminated bus with R_{source} less than cable Z_0	192
Figure D.5 – Waveforms on a source-terminated bus with R_{source} greater than cable Z_0 ..	192
Figure D.6 – Typical step voltage seen in ATA systems using an 80-conductor cable (measured at drive and host connectors during read).....	193
Figure D.7 – Typical step voltage seen in ATA systems using an 80-conductor cable (measured at host and drive connectors during write)	194
Figure D.8 – Positive crosstalk pulse during a falling edge.....	196
Figure D.9 – Reverse crosstalk waveform from reflected edge.....	196
Figure D.10 – Model of capacitive coupling.....	197
Figure D.11 – Waveforms resulting from capacitive coupling (at transmitter and receiver of aggressor and victim lines).....	198
Figure D.12 – Model of inductive coupling	199
Figure D.13 – Waveforms resulting from inductive coupling (at transmitter and receiver of aggressor and victim lines).....	199
Figure D.14 – Model of capacitive and inductive coupling.....	200
Figure D.15 – Waveforms resulting from mixed capacitive and inductive coupling (at transmitter and receiver of aggressor and victim lines)	201
Figure D.16 – Model of distributed coupling	202
Figure D.17 – Waveforms resulting from distributed coupling (at transmitter and receiver of aggressor and victim lines).....	202
Figure D.18 – Model of voltage divider for connector crosstalk formed by PCB and cable.....	204
Figure D.19 – Waveforms showing connector crosstalk dividing between PCB and cable	205
Figure D.20 – Model of ground bounce in IC package	207
Figure D.21 – Waveforms resulting from ground bounce (at transmitter and receiver of aggressor and victim lines).....	208
Figure D.22 – Simple RLC model of 40-conductor cable with all data lines switching	209
Figure D.23 – Output of simple RLC model: waveforms at source and receiving connectors	210
Figure D.24 – DST measurement for a line held low while all others are switching high (ch1 on DD3 at receiver, ch2 on DD11 at receiver)	210
Figure D.25 – DST measurement for all lines switching (ch1 at source, ch2 at receiver).....	211
Figure D.26 – Improved model of 40-conductor cable ringing with termination at IC	211

Figure D.27 – Improved model of 40-conductor cable ringing with termination at connector.....	212
Figure D.28 – Results of improved 40-conductor model with termination at IC versus connector.....	212
Figure D.29 – Results of improved 40-conductor model with source rise time of 1 ns, 5 ns and 10 ns.....	213
Figure D.30 – DMARDY- to final STROBE t_{RFS} synchronization.....	230
Figure D.31 – STROBE and DMARDY- at sender and recipient.....	234
Table 1 – PACKET delivered command sets.....	11
Table 2 – Byte order.....	27
Table 3 – Byte order.....	27
Table 4 – DC characteristics.....	29
Table 5 – AC characteristics.....	30
Table 6 – Driver types and required termination.....	32
Table 7 – Host transceiver configurations.....	33
Table 8 – System configuration for connection between devices and systems for all transfer modes.....	33
Table 9 – Typical series termination for Ultra DMA.....	34
Table 10 – Host or device 40-pin I/O header.....	36
Table 11 – 40-pin I/O cable connector.....	37
Table 12 – 40-pin I/O connector interface signals.....	38
Table 13 – 40-conductor cable configuration.....	39
Table 14 – 80-conductor cable electrical requirements.....	40
Table 15 – 80-conductor ribbon cable.....	40
Table 16 – 80-conductor cable configuration.....	41
Table 17 – Signal assignments for connectors grounding even conductors.....	42
Table 18 – Signal assignments for connectors grounding odd conductors.....	43
Table 19 – Device 4-pin power header.....	45
Table 20 – 4-pin power cable connector.....	46
Table 21 – 4-pin power connector pin assignments.....	46
Table 22 – Unitized connector.....	47
Table 23 – Unitized connector.....	48
Table 24 – 50-pin connector.....	49
Table 25 – Signal assignments for 50-pin 65 mm (2.5 in) form factor style connector.....	50
Table 26 – Signal assignments for 68-pin connector.....	51
Table 27 – 48 mm (1.8 in) 3.3 V parallel connector.....	55
Table 28 – 48 mm (1.8 in) 3.3 V parallel host connector.....	56
Table 29 – Pin assignments for the 48 mm (1.8 in) 3.3 V parallel connector.....	57
Table 30 – 95 mm (3.5 in) form factor.....	58
Table 31 – 65 mm (2.5 in) form factor.....	61
Table 32 – 65 mm (2.5 in) form factor connector location.....	64
Table 33 – 48 mm (1.8 in) 5 V parallel form factor.....	66
Table 34 – 48 mm (1.8 in) 5 V parallel form factor connector location.....	67
Table 35 – 48 mm (1.8 in) 3.3 V parallel form factor.....	69

Table 36 – 130 mm (5.25 in) HDD form factor.....	70
Table 37 – 130 mm (5.25 in) CD-ROM form factor.....	72
Table 38 – Interface signal name assignments.....	73
Table 39 – Cable type identification.....	77
Table 40 – Host detection of CBLID-.....	85
Table 41 – I/O registers.....	86
Table 42 – Device response to DIOW-/DIOR-.....	87
Table 43 – Device is not selected, DMACK- is not asserted.....	88
Table 44 – Device is selected, DMACK- is not asserted.....	89
Table 45 – Device is selected, DMACK- is asserted (for Multiword DMA only).....	90
Table 46 –Device 1 is selected and Device 0 is responding for Device 1.....	91
Table 47 – Device is in Sleep mode, DEVICE RESET is not implemented, DMACK- is not asserted.....	92
Table 48 – Device is in Sleep mode, DEVICE RESET is implemented, DMACK- is not asserted.....	93
Table 49 – Equations for parallel generation of a CRC polynomial.....	159
Table 50 – Register transfer to/from device.....	161
Table 51 – PIO data transfer to/from device.....	163
Table 52 – Multiword DMA data transfer.....	164
Table 53 – Ultra DMA data burst timing requirements.....	169
Table 54 – Ultra DMA data burst timing descriptions.....	170
Table 55 – Ultra DMA sender and recipient IC timing requirements.....	171
Table C.1 – Device detection of installed capacitor.....	186
Table C.2 – Results of device based cable detection if the host does not have the capacitor installed.....	186
Table C.3 – Results from using both host and device cable detection methods.....	187
Table C.4 – Results for all combinations of device and host cable detection methods.....	187
Table E.1 – Register functions and selection addresses except PACKET and SERVICE commands.....	242
Table E.2 – Register functions and selection addresses for PACKET and SERVICE commands.....	243